

# DIGITAL-LOGIC

smart embedded computers

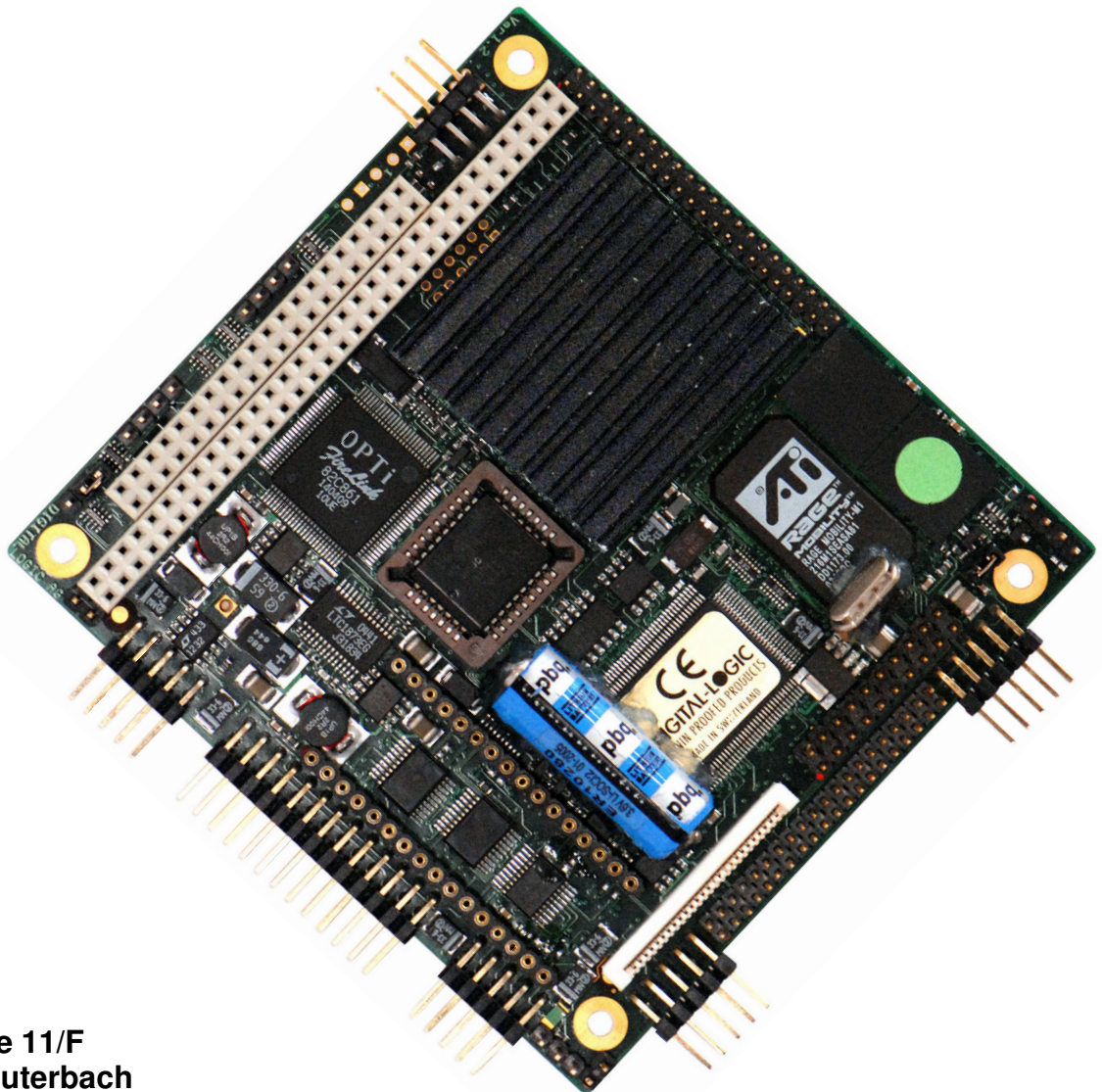
DETAILED USER MANUAL FOR:

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# MICROSPACE<sup>®</sup>

PC/104

# MSM586SEG/SEL/SL



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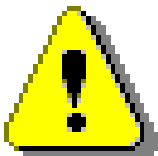
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## About this Manual and How to Use It

This manual is written for the original equipment manufacturer (OEM) who plans to build computer systems based on the single board MICROSPACE-PC. It is for integrators and programmers of systems based on the MICROSPACE-Computer family. This manual provides instructions for installing and configuring the board, and describes the system and setup requirements. This document contains information on hardware requirements, interconnections, and details of how to program the system. Please check the Product CD for further information and manuals.

## REVISION HISTORY:

Document Version	Date/Initials:	Modification: Remarks, News, Attention:
V0.1	09.2004 DAR	Initial version
V0.2	10.2004 DIM	Draft release
V0.3	10.2004 DAR	Current consumption, boot time, RS485, LAN
V1.0	11.2004 DAR	Final version
V1.0A	01.2005 DAR	RS485
V1.0B	03.2005 DAR	Minor corrections / VGA BIOS download / Chapter 4.5.2
V1.0C	06.2005 DAR	New dimensions, LAN BOOT, MSMSEG-DVICON added, ATI M1 LCD spec.
V1.0D	06.2006 DAR	Minor corrections
V1.0E	03.2007 DAR	Index structure / Jumper default settings
V1.2	04.2007 KUF	New manual structure
V1.2A	02.2009 WAS	Preface extended
<b>V1.2B</b>	<b>11.2009 WAS</b>	<b>Small corrections to BUS Signals</b>



### **Attention!**

1. All information in this manual, and the product, are subject to change without prior notice.
2. Read this manual prior to installation of the product.
3. Read the security information carefully prior to installation of the product.

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# 1. PREFACE

The information contained in this manual has been carefully checked and is believed to be accurate; it is subject to change without notice. Product advances mean that some specifications may have changed. DIGITAL-LOGIC AG assumes no responsibility for any inaccuracies, or the consequences thereof, that may appear in this manual. Furthermore, DIGITAL-LOGIC AG does not accept any liability arising from the use or application of any circuit or product described herein.

## 1.1. Trademarks

DIGITAL-LOGIC, DIGITAL-LOGIC-Logo, MICROSPACE, and smartModule are registered trademarks owned worldwide by DIGITAL-LOGIC AG, Luterbach (Switzerland). In addition, this document may include names, company logos, and registered trademarks which are, therefore, proprietary to their respective owners.

## 1.2. Disclaimer

DIGITAL-LOGIC AG makes no representations or warranties with respect to the contents of this manual, and specifically disclaims any implied warranty of merchantability or fitness, for any particular purpose. DIGITAL-LOGIC AG shall, under no circumstances, be liable for incidental or consequential damages or related expenses resulting from the use of this product, even if it has been notified of the possibility of such damage.

## 1.3. Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements wherever possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled. Final disposal of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

## 1.4. Who should use this Product

- Electrical engineers with know-how in PC-technology.
- Because of the complexity and the variability of PC-technology, we cannot guarantee that the product will work in any particular situation or set-up. Our technical support will try to help you find a solution.
- Pay attention to electrostatic discharges; use a CMOS protected workplace.
- Power supply must be OFF when working on the board or connecting any cables or devices.

## 1.5. Recycling Information

All components within this product fulfill the requirements of the RoHS (Restriction of Hazardous Substances Directive). The product is soldered with a lead free process.

## 1.6. Technical Support

1. Contact your local DIGITAL-LOGIC Technical Support, in your country.
2. Use the Internet Support Request form at <http://support.digitallogic.ch/> → embedded products → New Support Request

***Support requests are only accepted with detailed information about the product (i.e., BIOS-, Board-version)!***

## 1.7. Limited Two Year Warranty

DIGITAL-LOGIC AG guarantees the hardware and software products it manufactures and produces to be free from defects in materials and workmanship for two years following the date of shipment from DIGITAL-LOGIC AG, Switzerland. This warranty is limited to the original purchaser of the product and is not transferable.

During the two year warranty period, DIGITAL-LOGIC AG will repair or replace, at its discretion, any defective product or part at no additional charge, provided that the product is returned, shipping prepaid, to DIGITAL-LOGIC AG. All replaced parts and products become property of DIGITAL-LOGIC AG.

**Before returning any product for repair, direct customers of DIGITAL-LOGIC AG, Switzerland are required to register a RMA (Return Material Authorization) number in the Support Center at <http://support.digitallogic.ch/>**

**All other customers must contact their local distributors for returning defective materials.**

This limited warranty does not extend to any product which has been damaged as a result of accident, misuse, abuse (such as use of incorrect input voltages, wrong cabling, wrong polarity, improper or insufficient ventilation, failure to follow the operating instructions that are provided by DIGITAL-LOGIC AG or other contingencies beyond the control of DIGITAL-LOGIC AG), wrong connection, wrong information or as a result of service or modification by anyone other than DIGITAL-LOGIC AG. Nor if the user has insufficient knowledge of these technologies or has not consulted the product manuals or the technical support of DIGITAL-LOGIC AG and therefore the product has been damaged.

Empty batteries (external and onboard), as well as all other battery failures, are not covered by this manufacturer's limited warranty.

Except, as directly set forth above, no other warranties are expressed or implied, including, but not limited to, any implied warranty of merchantability and fitness for a particular purpose, and DIGITAL-LOGIC AG expressly disclaims all warranties not stated herein. Under no circumstances will DIGITAL-LOGIC AG be liable to the purchaser or any user for any damage, including any incidental or consequential damage, expenses, lost profits, lost savings, or other damages arising out of the use or inability to use the product.

## 1.8. Explanation of Symbols



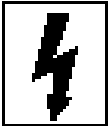
### **CE Conformity**

*This symbol indicates that the product described in this manual is in compliance with all applied CE standards.*



### **Caution, Electric Shock!**

*This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your equipment.*



### **Caution, Electric Shock!**

*This symbol and title warn of hazards due to electrical shocks (> 32V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your equipment.*



### **Warning, ESD Sensitive Device!**

*This symbol and title inform that electronic boards and their components are sensitive to Electro Static Discharge (ESD). In order to ensure product integrity at all times, care must always be taken while handling and examining this product.*



### **Attention!**

*This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your equipment.*



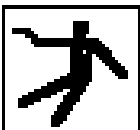
### **Note...**

*This symbol and title emphasize aspects the user should read through carefully for his, or her, own advantage.*



### **Warning, Heat Sensitive Device!**

*This symbol indicates a heat sensitive component.*



### **Safety Instructions**

*This symbol shows safety instructions for the operator to follow.*



*This symbol warns of general hazards from mechanical, electrical, and/or chemical failure. This may endanger your life/health and/or result in damage to your equipment.*

## 1.9. Applicable Documents and Standards

The following publications are used in conjunction with this manual. When any of the referenced specifications are superseded by an approved revision, that revision shall apply. All documents may be obtained from their respective organizations.

- Advanced Configuration and Power Interface Specification Revision 2.0c, August 25, 2003 Copyright © 1996-2003 Compaq Computer Corporation, Intel Corporation, Microsoft Corporation, Phoenix Technologies Ltd., Toshiba Corporation. All rights reserved. <http://www.acpi.info/>
- ANSI/TIA/EIA-644-A-2001: Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, January 1, 2001. <http://www.ansi.org/>
- ANSI INCITS 361-2002: AT Attachment with Packet Interface - 6 (ATA/ATAPI-6), November 1, 2002. <http://www.ansi.org/>
- ANSI INCITS 376-2003: American National Standard for Information Technology – Serial Attached SCSI (SAS), October 30, 2003. <http://www.ansi.org/>
- Audio Codec '97 Revision 2.3 Revision 1.0, April 2002 Copyright © 2002 Intel Corporation. All rights reserved. <http://www.intel.com/labs/media/audio/>
- Display Data Channel Command Interface (DDC/CI) Standard (formerly DDC2Bi) Version 1, August 14, 1998 Copyright © 1998 Video Electronics Standards Association. All rights reserved. <http://www.vesa.org/summary/sumddcci.htm>
- ExpressCard Standard Release 1.0, December 2003 Copyright © 2003 PCMCIA. All rights reserved. <http://www.expresscard.org/>
- IEEE 802.3-2002, IEEE Standard for Information technology, Telecommunications and information exchange between systems—Local and metropolitan area networks—Specific requirements – Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications. <http://www.ieee.org>
- IEEE 802.3ae (Amendment to IEEE 802.3-2002), Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications, Amendment: Media Access Control (MAC) Parameters, Physical Layers, and Management Parameters for 10 GB/s Operation. <http://www.ieee.org>
- Intel Low Pin Count (LPC) Interface Specification Revision 1.1, August 2002 Copyright © 2002 Intel Corporation. All rights reserved. <http://developer.intel.com/design/chipsets/industry/lpc.htm>
- PCI Express Base Specification Revision 1.1, March 28, 2005, Copyright © 2002-2005 PCI Special Interest Group. All rights reserved. <http://www.pcisig.com/>
- PCI Express Card Electromechanical Specification Revision 1.1, March 28, 2005, Copyright © 2002-2005 PCI Special Interest Group. All rights reserved. <http://www.pcisig.com/>
- PCI Local Bus Specification Revision 2.3, March 29, 2002 Copyright © 1992, 1993, 1995, 1998, 2002 PCI Special Interest Group. All rights reserved. <http://www.pcisig.com/>
- PCI-104 Specification, Version V1.0, November 2003. All rights reserved. <http://www.pc104.org>
- PICMG® Policies and Procedures for Specification Development, Revision 2.0, September 14, 2004, PCI Industrial Computer Manufacturers Group (PICMG®), 401 Edgewater Place, Suite 500, Wakefield, MA 01880, USA, Tel: 781.224.1100, Fax: 781.224.1239. <http://www.picmg.org/>
- Serial ATA: High Speed Serialized AT Attachment Revision 1.0a January 7, 2003 Copyright © 2000-2003, APT Technologies, Inc, Dell Computer Corporation, Intel Corporation, Maxtor Corporation, Seagate Technology LLC. All rights reserved. <http://www.sata-io.org/>

- Smart Battery Data Specification Revision 1.1, December 11, 1998. [www.sbs-forum.org](http://www.sbs-forum.org)
- System Management Bus (SMBus) Specification Version 2.0, August 3, 2000 Copyright © 1994, 1995, 1998, 2000 Duracell, Inc., Energizer Power Systems, Inc., Fujitsu, Ltd., Intel Corporation, Linear Technology Inc., Maxim Integrated Products, Mitsubishi Electric Semiconductor Company, Power-Smart, Inc., Toshiba Battery Co. Ltd., Unitrode Corporation, USAR Systems, Inc. All rights reserved. <http://www.smbus.org/>
- Universal Serial Bus Specification Revision 2.0, April 27, 2000 Copyright © 2000 Compaq Computer Corporation, Hewlett-Packard Company, Intel Corporation, Lucent Technologies Inc., Microsoft Corporation, NEC Corporation, Koninklijke Philips Electronics N.V. All rights reserved. <http://www.usb.org/>

## 1.10. For Your Safety

Your new DIGITAL-LOGIC product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long, fault-free life. However, this life expectancy can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and for the correct operation of your new DIGITAL-LOGIC product, please comply with the following guidelines.



### ***Attention!***

All work on this device must only be carried out by sufficiently skilled personnel.



### ***Caution, Electric Shock!***

Before installing your new DIGITAL-LOGIC product, always ensure that your mains power is switched off. This applies also to the installation of piggybacks or peripherals. Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltage before performing work.



### ***Warning, ESD Sensitive Device!***

Electronic boards and their components are sensitive to static electricity. In order to ensure product integrity at all times, be careful during all handling and examinations of this product.

## 1.11. RoHS Commitment

DIGITAL-LOGIC AG is committed to develop and produce environmentally friendly products according to the Restriction of Hazardous Substances (RoHS) Directive (2002/95/EC) and the Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) established by the European Union. The RoHS directive was adopted in February 2003 by the European Union and came into effect on July 1, 2006. It is not a law but a directive, which restricts the use of six hazardous materials in the manufacturing of various types of electronic and electrical equipment. It is closely linked with the Waste Electrical and Electronic Equipment Directive (WEEE) 2002/96/EC, which has set targets for collection, recycling and recovery of electrical goods and is part of a legislative initiative to solve the problem of huge amounts of toxic e-waste.

Each European Union member state is adopting its own enforcement and implementation policies using the directive as a guide. Therefore, there could be as many different versions of the law as there are states in the EU. Additionally, non-EU countries like China, Japan, or states in the U.S. such as California may have their own regulations for green products, which are similar, but not identical, to the RoHS directive.

RoHS is often referred to as the "lead-free" directive but it restricts the use of the following substances:

- Lead
- Mercury
- Cadmium
- Chromium VI
- PBB and PBDE

The maximum allowable concentration of any of the above mentioned substances is 0.1% (except for Cadmium, which is limited to 0.01%) by weight of homogeneous material. This means that the limits do not apply to the weight of the finished product, or even to a component but to any single substance that could (theoretically) be separated mechanically.

### **1.11.1. RoHS Compatible Product Design**

All DIGITAL-LOGIC standard products comply with RoHS legislation.

Since July 1, 2006, there has been a strict adherence to the use of RoHS compliant electronic and mechanical components during the design-in phase of all DIGITAL-LOGIC standard products.

### **1.11.2. RoHS Compliant Production Process**

DIGITAL-LOGIC selects external suppliers that are capable of producing RoHS compliant devices. These capabilities are verified by:

1. A confirmation from the supplier indicating that their production processes and resulting devices are RoHS compliant.
2. If there is any doubt of the RoHS compliancy, the concentration of the previously mentioned substances in a produced device will be measured. These measurements are carried out by an accredited laboratory.

### **1.11.3. WEEE Application**

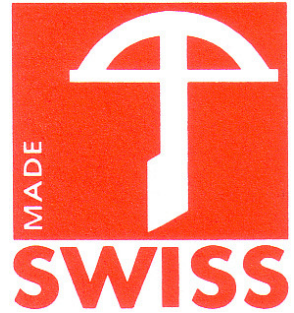
The WEEE directive is closely related to the RoHS directive and applies to the following devices:

- Large and small household appliances
- IT equipment
- Telecommunications equipment (although infrastructure equipment is exempt in some countries)
- Consumer equipment
- Lighting equipment – including light bulbs
- Electronic and electrical tools
- Toys, leisure and sports equipment
- Automatic dispensers

It does not apply to fixed industrial plants and tools. The compliance is the responsibility of the company that brings the product to market, as defined in the directive. Components and sub-assemblies are not subject to product compliance. In other words, since DIGITAL-LOGIC does not deliver ready-made products to end users the WEEE directive is not applicable for DIGITAL-LOGIC. Users are nevertheless encouraged to properly recycle all electronic products that have reached the end of their life cycle.

## 1.12. Swiss Quality

- 100% Made in Switzerland
- DIGITAL-LOGIC is a member of "Swiss-Label"
- This product was **not** manufactured by employees earning piecework wages
- This product was manufactured in humane work conditions
- All employees who worked on this product are paid customary Swiss market wages and are insured
- ISO 9000:2001 (quality management system)



## 1.13. The Swiss Association for Quality and Management Systems

The Swiss Association for Quality and Management Systems (SQS) provides certification and assessment services for all types of industries and services. SQS certificates are accepted worldwide thanks to accreditation by the Swiss Accreditation Service (SAS), active membership in the International Certification Network, IQNet, and co-operation contracts/agreements with accredited partners.

[www.sqs.ch](http://www.sqs.ch)

The SQS Certificate ISO 9001:2000 has been issued to DIGITAL-LOGIC AG, the entire company, in the field of development, manufacturing and sales of embedded computer boards, embedded computer modules and computer systems. The certification is valid for three years at which time an audit is performed for recertification.

## 2. OVERVIEW

### 2.1. Standard Features

The MICROSPACE PC/104 is a miniaturized modular device incorporating the major elements of a PC/AT compatible computer. It includes standard PC/AT compatible elements, such as:

MSM586SEG	Version with:	LAN and graphic output (ATI M1 EOL)
MSM586SL	Version <i>without</i> :	LAN, graphic output or USB
MSM586SEL	Version with:	LAN only

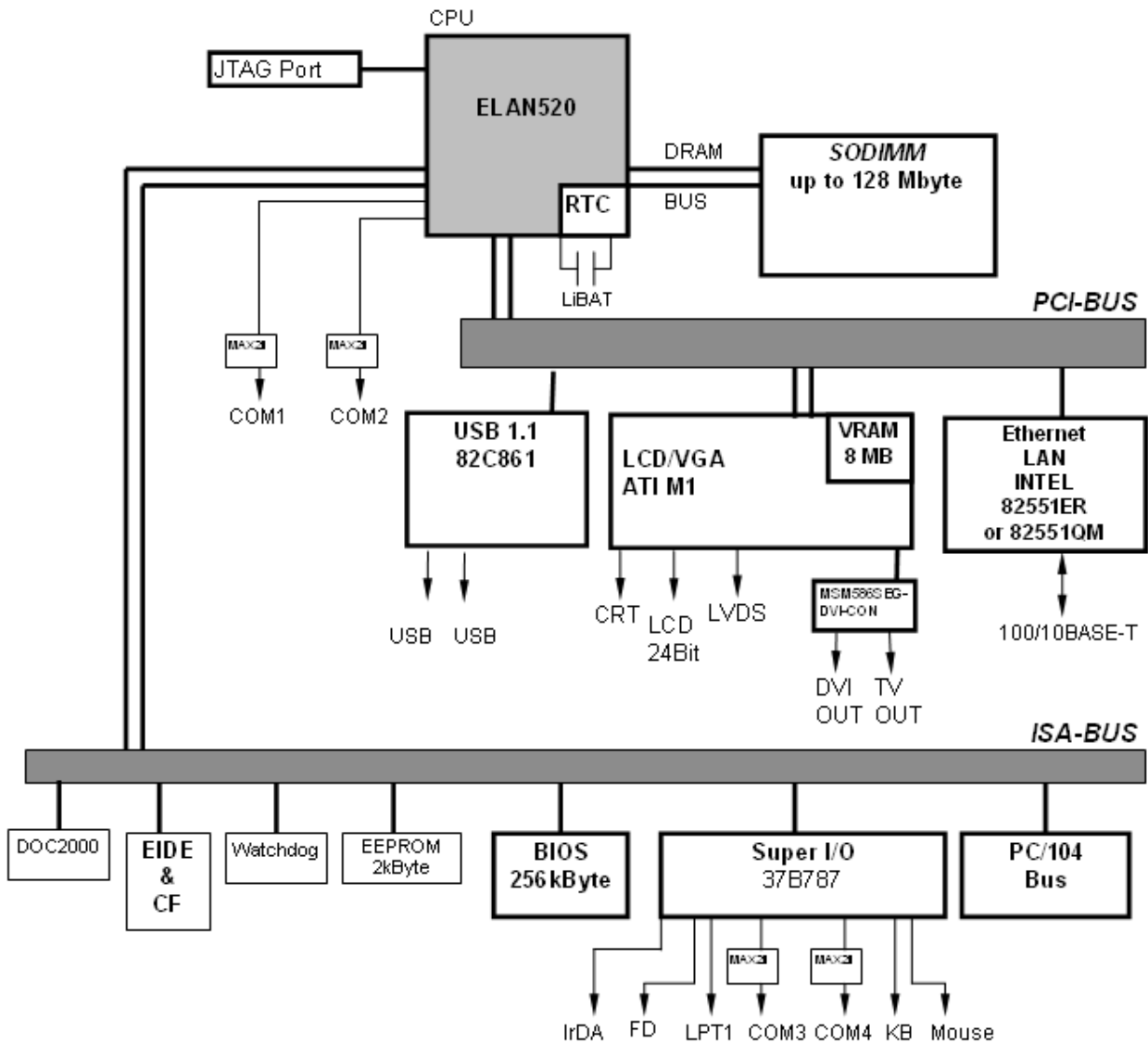
- Powerful ELAN520 133MHz
- BIOS ROM
- SODIMM 16 to 128 MBytes 70ns (32bit device, no ECC supported)
- Timers
- DMA
- Real-time clock with CMOS-RAM and battery buffer
- LPT1 parallel port
- COM1, COM2, COM3, COM4 serial ports
- Speaker interface
- AT-keyboard interface or PS/2-keyboard interface
- PS/2 mouse interface
- Floppy disk interface
- AT-IDE hard disk interface
- VGA/LCD video interface
- PC/104 embedded BUS
- 2 Ports USB 1.1 interface (no legacy support)

### 2.2. Unique Features

The MICROSPACE PC/104 includes all standard PC/AT functions plus unique DIGITAL-LOGIC AG enhancements, such as:

- Single 5Volt supply
- LAN Ethernet 82551ER/QM
- DOC2000
- Compact card type 1
- Watchdog
- Power-fail
- EEPROM for setup and configuration
- Core- and VGA BIOS downloadable
- JTAG for debugging with CADUL KIT
- **(NO** power management functions)
- UL approved parts

### 2.3. Block Diagram



## 2.4. Specifications

CPU	
CPU	AMD ELAN520 – 133MHz
Compatibility	8086-Pentium
1 <sup>st</sup> Level Cache	16k data and 16k code
2 <sup>nd</sup> Level Cache	None
Socket	BGA
Clock	133MHz
FSB	33MHz
Power Management	None
FPU	Integrated

Chipset	
Northbridge	AMD ELAN520
Southbridge	AMD ELAN520
LAN	82551ER INTEL [ <i>only on the MSM586SEL/SEG</i> ]
Audio	Not onboard
Firewire IEEE1394	Not onboard
Video	ATI Mobility-M1 EOL-product (8MB) [ <i>only on the MSM586SEG</i> ]
Frame grabber/TV-Input	Not onboard

Memory	
Main Memory	SDRAM, 32bit, up to 128MByte in one SODIMM144 socket
Flash-BIOS	256kByte Flash
Setup EEPROM	2kByte for CMOS-backup in battery-less applications
Flash-Video BIOS	Serial-Flash
Video RAM	Separate 2MByte

Video Controller	
<b><i>only on the MSM586SEG product</i></b>	
Controller	ATI Mobility-M1 (Video controller EOL since Feb. 2007)
Video Memory	8MByte SDRAM
Channel 1	CRT VGA up to 1280x1024 pixels
Channel 2	LCD / TV-OUT with external adapter print
Boot up-Resolution	DDC Support for EDID standard 2.0 Resolution 640x480 / 800x600 / 1024x768 / 1280x1024
2D-Graphics	Integrated accelerator
3D-Graphics	Integrated accelerator

External Interfaces	
Video Interfaces	CRT1, LCD for TFT, TV-Out [ <i>only on the MSM586SEG</i> ]
USB	V1.1 (without legacy support) [ <i>only on the MSM586SEL/SEG</i> ]
LPT1	Internal
COM1	RS232 (Optional RS485)
COM2	RS232 (Optional RS485)
COM3	RS232 (Optional RS485)
COM4	RS232 (Optional RS485)
Keyboard	PS/2
Mouse	PS/2
Floppy	26pin FCC Interface for TEAC Mini-floppy
Hard Disk	1 channel 44pin RM2.0mm ATAIDE-cable
Speaker	0.1Watt Speaker
LAN	100/10Mbit/s [ <i>only on the MSM586SEL and MSM586SEG</i> ]

Power Supply	
Input	Nominal 5V, Tolerance +/- 3%
Protection	Not integrated, EMI filtered must be added externally
Specification	Nominal 25Watt, min. 10Watt, depending on the peripherals

Power Consumption	
At 5V	Refer to Section 4.1 in this manual
Standby	Not available
Power-off	0mA

Physical Characteristics	
	<b>PC/104</b>
Dimensions	Length: 91mm Depth: 96mm Height: 25mm
Weight	170gr

Operating Environment	
Relative Humidity	5-90% non-condensing IEC68-2-30 at -20° to +50°C, operating
Vibration, operating	IEC68-2-6 10-50Hz, 0.075mm and 55-500Hz, 1.0G
Vibration, non-operating	IEC68-2-6 10-50Hz, 0.15mm and 55-500Hz, 2.0G
Shock, operating	IEC68-2-27 10G, 11ms ½ sine
Shock, non-operating	IEC68-2-27 50G, 11ms, ½ sine
Altitude	IEC68-2-13 4571 meter, operating
Temperature, operating	IEC68-2-1,2,14 Standard -25°C to +70°C
Extended Temperature option	MIL-810-501/502 Extended temperature -40°C to +85°C
Temperature, storage	IEC68-2-1,2,14 -65°C to +125°C ★

★ The back-up battery is limited on -40°C to +85°C operating and storage temperature!

EMI / EMC Tests	If all signals are externally filtered and assembled inside a closed metallic case!
EMC emission EN61000-6-2:2001	
Conducted disturbance	EN55022 Class B
Radiated disturbance	EN55022 Class B
EMC immunity EN61000-6-2	
Electrostatic discharge (ESD)	EN61000-4-2 Voltage = 4kV contact / 8kV air Criteria A
Radiated RF-Field	EN61000-4-3 Level = 10V/m Criteria A
Electrical fast transients (Burst)	EN61000-4-4 Grade 2: DC-Power lines = 1000V (5/50ns) Grade 2: AC-Power lines = 2000V (5/50ns) Grade 2: Signal lines = 500V (5/50ns) Criteria B
Surge	EN61000-4-5 Grade 2: DC-Power lines = 1kV (1.2/50us) Grade 2: AC-Power lines = 2kV (1.2/50us) Criteria B
Conducted disturbances	EN61000-4-6 Voltage = 10V coupled by case Criteria A

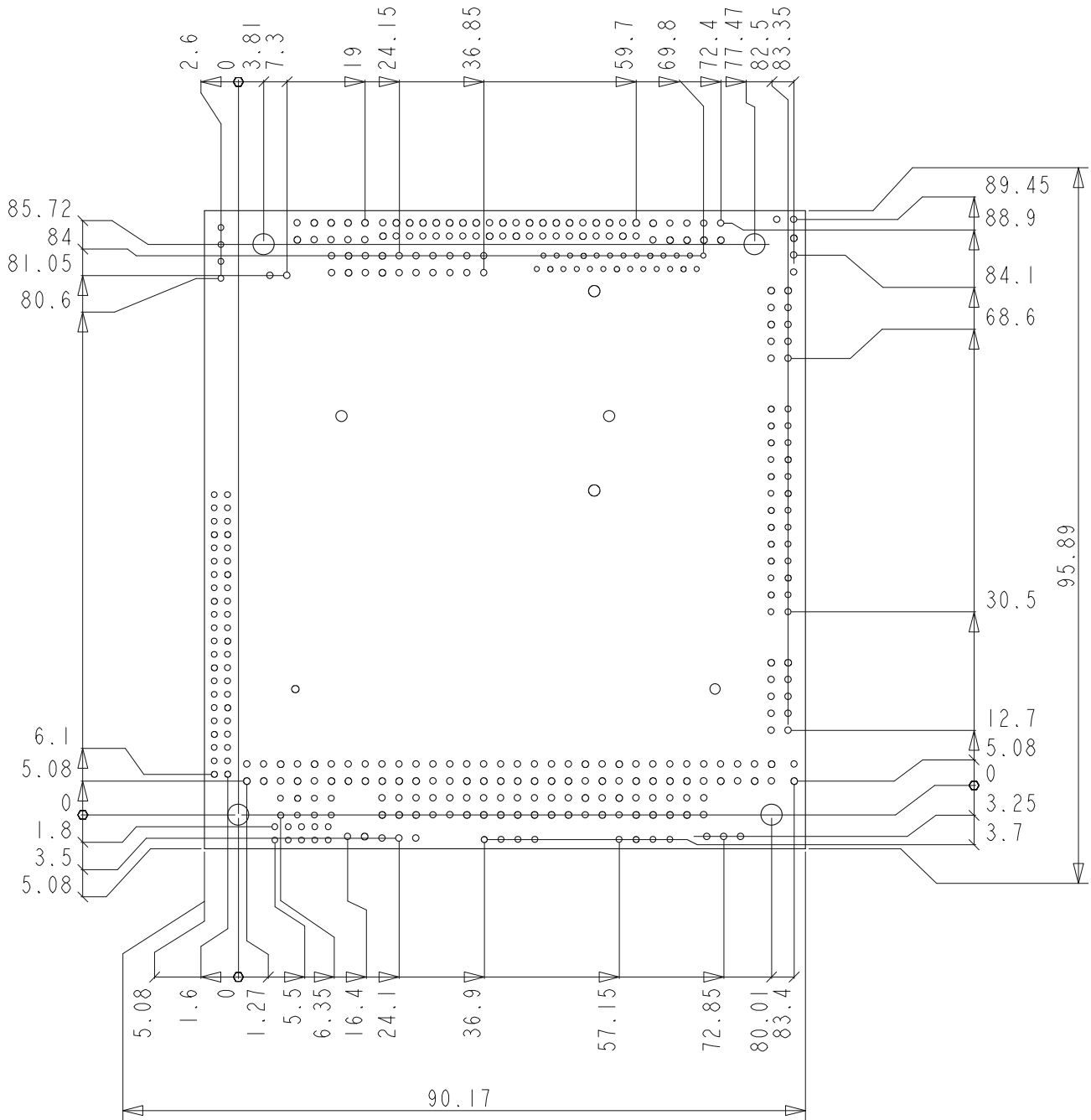
Security	
e1	Not planned
UL	Not planned
ETS 301	Not planned
CE/SEV	Yes
Safety	AR385-16

**Note...**

All information is subject to change without notice.

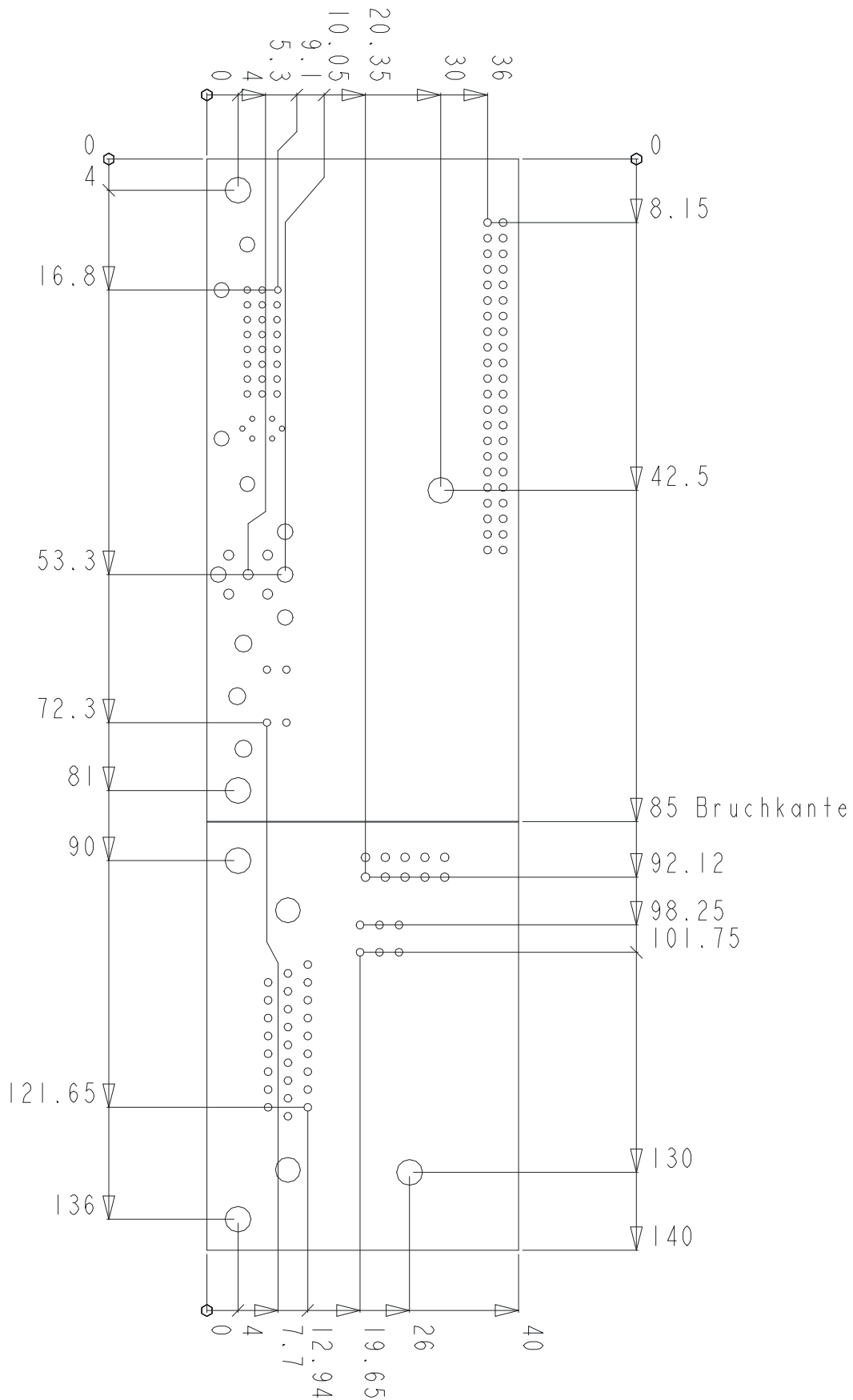
## 2.5. Mechanical Dimensions

### 2.5.1. Version 1.1 / 1.2



MSM586SEG Version V1.2 Unit: mm (millimeter) Tolerance: +/- 0.1mm  
Date: 11.04.2005 Author: BRR

2.5.2. MSMSEG-DVICON



## 2.6. Incompatibilities to a standard PC/AT



### **Attention!**

Please pay particular attention to the following:

1. **Do not use the internal COM1/2 of the ELAN520 in FIFO-Mode. AMD Errata**  
Some bits are lost in certain configurations of FIFO-Mode in extended temperature ranges.  
*Solution:* Use the COM3/4 for FIFO Mode. Use a None-FIFO-Driver!
2. PRETEC Cflash: not working with the Toshiba controller (ACT...)  
working fine with the HITACHI Controller (ACH...)  
a bug fixed by PRETEC
3. LINUX need a BIOS without INT15 service, otherwise the DRAM-capacity is not well reported. Last observation of this was with BIOS V1.24.
4. USB works without legacy support. That means there is no USB function in the BIOS setup, no boot function for USB drives and drivers are needed in all OS.

## 2.7. Related Application Notes

Application Notes are available at <http://www.digitallogic.com> → support, or on any DIGITAL-LOGIC Application CD.

#	Description

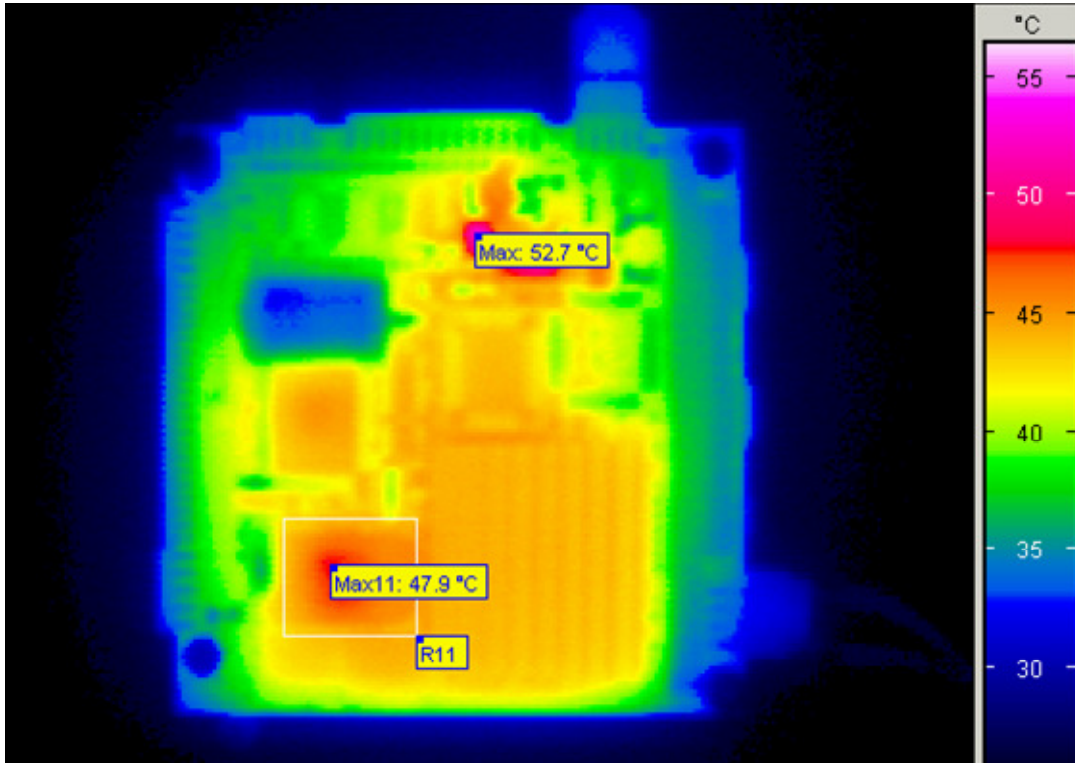
## 2.8. Examples of Ordering Codes

Part / Option	Part Nr.	Description
MSM586SL	801344	Low cost version without: LAN, VGA-Grafic
MSM586SEL	801380	Standard version with: LAN
MSM586SEG	801370	Standard version with: LAN and VGA-Grafic (EOL product)
Option -L+	807006	PC/104-Plus with long connector
Option -P+	807005	PC/104-Plus with short connector
Option -CF	807007	CompactFlash socket (without Option -L)
MSM-CK	802605	MSM586 PC/104-cable kit
MSFLOPPY	891001	3.5" Micro-floppy drive (26pin)
MSFDCK	802600	Micro-floppy cable (26pin)
MSM586SEG-DK	801378	Development kit

*These are only examples; for current ordering codes, please see the current price list.*

## 2.9. Thermoscan

MSM586SEG V1.1, 133MHz, 60 min.



## 2.10. High Frequency Radiation (to meet EN55022 &EN61000)

Since the PC/104 CPU modules are very highly integrated embedded computers, peripheral lines are not protected against radiation from the high frequency spectrum. To meet a typical EN55022 requirement, all peripherals that go outside of the computer case must be externally filtered.

Typical signals that must be filtered:

Keyboard:	KBCLK, KBDATA and VCC
Mouse:	MSCLK, MSDATA and VCC
COM1/2/3/4:	All serial signals must be filtered
LPT:	All parallel signals must be filtered
CRT:	Red, blue, green, hsync and vsynch must be filtered

Typical signals that must not be filtered, since they are used internally:

IDE:	Connected to the hard disk
Floppy:	Connected to the floppy
LCD:	Connected to the internal LCD

### 2.10.1. For Peripheral Cables:

Use a filtered version for all DSUB connectors. Select the filter specifications carefully. Place the filtered DSUB connector directly on the front side and be sure that the shielding makes good contact with the case.

9pin	DSUB connector from AMPHENOL:	FCC17E09P	820pF
25pin	DSUB connector from AMPHENOL:	FCC17B25P	820pF

### 2.10.2. For Stack-Through Applications:

On each peripheral signal line that goes outside the computer case, place a serial inductivity followed by a grounded capacitor of 100pF to 1000pF. In this case, no filtered connectors are needed. Place the filter directly under or behind the onboard connector.

Serial Inductivity:	TDK HF50ACB321611-T	100Mhz, 500mA, 1206 Case
Ground capacitor:	Ceramic Capacitor with 1000pF	

### 2.10.3. Power Supply:

We recommend using the MSMPS104 PSU.

## 2.11. Battery Lifetime

Battery specifications		Lowest temp. -40 °C	Nominal temp. +20 °C	Highest temp. +85 °C
Manufacturer	pba			
Type	ER10280 from pbq			
Capacity versus temp.	10uA	360mAh	400mAh	220mAh
Voltage versus temp.	10uA	3.6V	3.6V	Ca. 3.6V
Open circuit temperature			Up to 3.7V	
Nominal values	3.6V / 400mAh @ 0.5mA / -55°C... ~+85°C			

*Information is taken from the datasheet of the ER10280.*

Product	Temperature °C	Battery voltage (min. 2.6V) V	VCC (+12V) switched ON µA	VCC (+12V) switched off µA
Battery current	+25 °C	3.6	0	10
Battery lifetime	+25 °C		> 3.5 years	> 3.5 years

### 2.11.1. External Battery Assembly:

If the customer wants to connect an external battery (check for the appropriate connector in the chapter "Description of the Connectors") some precautions must be taken:

- Do not use a rechargeable battery – the battery is prohibited from charging.
- The RTC device defines a voltage level of 3-3.6V, so use an external battery within this range (inclusive of the diode which is already assembled onboard).

The system integrator is responsible for checking the discharging current of a newly connected RT battery, to be sure that the back-up battery is working correctly. The discharging current should be lower than 5µA, if the computer is switched off. If the computer is running, the discharging current must fall below 1µA.



#### **Attention!**

For systems that already have an onboard battery, if an external battery is to be connected, then the onboard battery **must** be removed first.

## 3. BUS SIGNALS

### 3.1. PC104 BUS



**Note...**

Not all of the signals are available on this board (please see the chapter "Description of the Connectors").

**AEN, output**

Address Enable: used to degate the microprocessor and other devices from the I/O channel to allow DMA transfers to take place. **low = CPU Cycle, high = DMA Cycle**

**BALE, output**

Address Latch Enable: provided by the bus controller and used on the system board to latch valid addresses and memory decodes from the microprocessor. This signal is used so that devices on the bus can latch LA17-23. The SA0-19 address lines latch internally according to this signal. BALE is forced high during DMA cycles.

**/DACK[0-3, 5-7], output**

DMA Acknowledge: 0 to 3 and 5 to 7 are used to acknowledge DMA requests (DRQ0 through DRQ7). They are **active low**. This signal indicates that the DMA operation can begin.

*Not available on ELAN520 (DACK5-7)*

**DRQ[0-3, 5-7], input**

DMA Requests: 0 through 3 and 5 through 7 are asynchronous channel requests used by peripheral devices and the I/O channel microprocessors to gain DMA service (or control of the system). A request is generated by bringing a DRQ line to an active level. A DRQ line must be held high until the corresponding DMA Request Acknowledge (DACK/) line goes active. DRQ0 through DRQ3 will perform 8bit DMA transfers; DRQ5-7 are used for 16 accesses.

*Not available on ELAN520 (DRQ5-7)*

**/IOCHCK, input**

IOCHCK/: provides the system board with parity (error) information about memory or devices on the I/O channel. **low = parity error, high = normal operation**

**IOCHRDY, input**

I/O Channel Ready: pulled low (not ready) by a memory or I/O device to lengthen I/O or memory cycles. Any slow device using this line should drive it low immediately upon detecting its valid address and a Read or Write command. Machine cycles are extended by an integral number of one clock cycle (67 nanoseconds). This signal should be held in the range of 125-15600nS. **low = wait, high = normal operation**

**/IOCS16, input**

I/O 16 Bit Chip Select: signals the system board that the present data transfer is a 16bit, 1 wait-state, I/O cycle. It is derived from an address decode. /IOCS16 is **active low** and should be driven with an open collector (300 Ohm pull-up) or tri-state driver capable of sinking 20mA. The signal is driven based only on SA0-SA15 (not /IOR or /IOW) when AEN is not asserted. In the 8bit I/O transfer, the default transfers a 4 wait-state cycle.

**/IOR, input/output**

I/O Read: instructs an I/O device to drive its data onto the data bus. It may be driven by the system microprocessor or DMA controller, or by a microprocessor or DMA controller resident on the I/O channel. This signal is active low.

**/IOW, input/output**

I/O Write: instructs an I/O device to read the data on the data bus. It may be driven by any microprocessor or DMA controller in the system. This signal is **active low**.

**IRQ [3-7, 9-12, 14, 15], input**

These signals are used to tell the microprocessor that an I/O device needs attention. An interrupt request is generated when an IRQ line is **raised from low to high**. The line must be held high until the microprocessor acknowledges the interrupt request.

**/Master, input**

This signal is used with a DRQ line to gain control of the system. A processor or DMA controller on the I/O channel may issue a DRQ to a DMA channel in cascade mode and receive a /DACK.

*Not available on ELAN520*

**/MEMCS16, input**

MEMCS16 Chip Select: signals the system board if the present data transfer is a 1 wait-state, 16bit, memory cycle. It must be derived from the decode of LA17 through LA23. /MEMCS16 should be driven with an open collector (300 Ohm pull-up) or tri-state driver capable of sinking 20mA.

**/MEMR, input/output**

These signals instruct the memory devices to drive data onto the data bus. /MEMR is active on all memory read cycles. /MEMR may be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/O channel wishes to drive /MEMR, it must have the address lines valid on the bus for one system clock period before driving /MEMR active. These signals are **active low**.

**/MEMW, input/output**

These signals instruct the memory devices to store the data present on the data bus. /MEMW is active in all memory read cycles. /MEMW may be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/O channel wishes to drive /MEMW, it must have the address lines valid on the bus for one system clock period before driving /MEMW active. Both signals are **active low**.

**OSC, output**

Oscillator (OSC): a high-speed clock with a 70 nanosecond period (14.31818 MHz). This signal is not synchronous with the system clock. It has a 50% duty cycle. OSC starts 100 $\mu$ s after reset is inactive.

**RESETDRV, output**

Reset Drive: used to reset or initiate system logic at power-up time or during a low line-voltage outage. This signal is **active high**. When the signal is active all adapters should turn off or tri-state all drivers connected to the I/O channel. This signal is driven by the permanent Master.

**/REFRESH, input/output**

These signals are used to indicate a refresh cycle and can be driven by a microprocessor on the I/O channel. These signals are **active low**.

*ELAN520 pulls up this signal with 1k $\Omega$*

**SA0-SA19, LA17 - LA23 input/output**

Address bits 0 through 19 are used to address memory and I/O devices within the system. These 20 address lines, allow access of up to 1MBytes of memory. SA0 through SA19 are gated on the system bus when BALE is high and are latched on the falling edge of BALE. LA17 to LA23 are not latched and addresses the full 16MByte range. These signals are generated by the microprocessors or DMA controllers. They may also be driven by other microprocessor or DMA controllers that reside on the I/O channel. The SA17-SA23 are always LA17-LA23 address timings for use with the MSCS16 signal. This is advanced AT96 design. The timing is selectable with jumpers L $x$ x or S $x$ x.

**/SBHE, input/output**

Bus High Enable (system): indicates a transfer of data on the upper byte of the data bus, XD8 through XD15. Sixteen-bit devices use /SBHE to condition data-bus buffers tied to XD8 through XD15.

**SD[0-15], input/output**

These signals provide bus bits 0 through 15 for the microprocessor, memory, and I/O devices. D0 is the least significant bit and D15 is the most significant bit. All 8bit devices on the I/O channel should use D0 through D7 for communications to the microprocessor. The 16bit devices will use D0 through D15. To support 8bit devices, the data on D8 through D15 will be gated to D0 through D7 during 8bit transfers to these devices; 16bit microprocessor transfers to 8bit devices will be converted to two 8bit transfers.

**/SMEMR, input/output**

These signals instruct the memory devices to drive data onto the data bus for the first MByte. /SMEMR is active on all memory read cycles. /SMEMR may be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/O channel wishes to drive /SMEMR, it must have the address lines valid on the bus for one system clock period before driving /SMEMR active. The signal is **active low**.

**/SMEMW, input/output**

These signals instruct the memory devices to store the data present on the data bus for the first MByte. /SMEMW is active in all memory read cycles. /SMEMW may be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/O channel wishes to drive /SMEMW, it must have the address lines valid on the bus for one system clock period before driving /SMEMW active. Both signals are **active low**.

**SYSCLK, output**

This is an 8MHz system clock. It is a synchronous microprocessor cycle clock with a cycle time of 167 nanoseconds. The clock has a 66% duty cycle. This signal should only be used for synchronization.

*Available on ELAN520 since board Version 2.2.*

**TC, output**

Terminal Count: provides a pulse when the terminal count for any DMA channel is reached. The TC completes a DMA-Transfer. This signal is expected by the onboard floppy disk controller. Do not use this signal, because it is internally connected to the floppy controller.

**/OWS, input**

The Zero Wait State (/OWS) signal tells the microprocessor that it can complete the present bus cycle without inserting any additional wait cycles. In order to run a memory cycle to a 16bit device without wait cycles, /OWS is derived from an address decode gated with a Read or Write command. In order to run a memory cycle to an 8bit device with a minimum of one-wait states, /OWS should be driven active one system clock after the Read or Write command is active, gated with the address decode for the device. Memory Read and Write commands to an 8bit device are active on the falling edge of the system clock. /OWS is **active low** and should be driven with an open collector or tri-state driver capable of sinking 20mA.

*Not available on ELAN520*

**12V, +/- 5%**

This signal is used only for the flat panel supply.

**GROUND = 0V**

This is used for the entire system.

**VCC, +5V +/- 0.25V**

This signal is used for logic and hard/floppy disk supply.

**For further information about PC/104 and PC/104plus, please refer to the PC/104 Specification Manual which is available on the internet: <http://www.digitallogic.com> (manuals).**

## 3.2. BUS Levels

The bus currents are as follows:

Output Signals	IOH	IOL
D0-D16	8 mA	8 mA
A0-A23	8 mA	8 mA
MR, MW, IOR, IOW, RES, ALE, AEN, C14	8 mA	8 mA
DACKx, DRQx, INTx, PSx, OPW	8 mA	8 mA

Output Signals	Logic Family	Voltage
Input Signals:	ABT-Logic ViH (min.) = 2.15 V	ABT-Logic Vil (max.) = 0.85 V

## 4. DETAILED SYSTEM DESCRIPTION

This system has a system configuration based on the ISA architecture. Check the I/O and the Memory maps later in this chapter.

### 4.1. Power Requirements

The power is connected through the PC/104 power connector or the separate power connector on the board. The supply uses only +5Volts and a ground connection.



#### **Warning!**

Be sure the power plug is wired correctly before supplying power to the board! A built-in diode protects the board against reverse polarity.

**Tolerance of the 5V supply:** 5Volt  $\pm 5\%$ ; the power-fail signal starts at  $\pm 10\%$  of the 5V norm and generates a reset status for the MICROSPACE PC.



#### **Attention!**

With the hard disk connected to the IDE 44pin interface, the power requirement is high. The peak current must be enough to spin up the HD motor. The typical spin-up current of the hard disk is 0.8-1.5Amp at 5V. Too little current will drop the voltage to under 5Volt for a short time. Due to this undervoltage, the system or the hard disk stops or falters. The VGA may also be "snowy".

The precise power requirements of the MICROSPACE MSM586SEV depend on a number of factors, including which functions are present on the board and which peripherals are connected to the board's I/O port. For example, AT-keyboards draw their power from the keyboard connector on the MICROSPACE MSM586SEV board, and therefore add keyboard current to the total power drawn by the board from its power supply.

**Test environment for the power consumption measurement:**

## Peripherals:

Hard disk Hitachi Mod-DK23AA-60  
 Monitor Compaq Mod-460  
 CompactFlash SanDisk 64MB  
 DOC2000 16MB  
 PS/2-KB Logitech Mod-iTouch Keyboard  
 PS/2-MS Logitech Mod-M-CAA43  
 Floppy TEAC Mod-FD-05HF

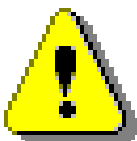
## Software:

MS-DOS V6.22  
 Win98SE Second Edition  
 HCT for Win 98 v8.1 Performance test tool from Microsoft.

**Current consumption @ 5Volt supply at -40°C/+25°C/+85°C:**

Mode	Memory	DLAG-Nr.	-30°C	+25°C	+85°C
MSM586SEG			[mA]	[mA]	[mA]
<b>DOSv6.22:</b> A:\	16MB	890645 SDRAM	1190	1100	1123
	32MB	890655 SDRAM	1047	1087	1092
	64MB	890654 SDRAM	1082	1089	1099
	128MB	890656 SDRAM	1050	1091	1089
<b>DOSv6.22:</b> EDIT running autoexec.bat	16MB	890645 SDRAM	1072	1080	1103
	32MB	890655 SDRAM	1048	1080	1045
	64MB	890654 SDRAM	1105	1200	1233
	128MB	890656 SDRAM	987	1090	1120
<b>Win98SE:</b> Desktop	16MB	890645 SDRAM	1060	1100	1099
	32MB	890655 SDRAM	1062	1120	1160
	64MB	890654 SDRAM	1058	1100	1170
	128MB	890656 SDRAM	1055	1100	1156
<b>Win98SE:</b> HCT	16MB	890645 SDRAM	1372	1490	1486
	32MB	890655 SDRAM	1365	1490	1144
	64MB	890654 SDRAM	1355	1470	1456
	128MB	890656 SDRAM	1332	1465	1439

Power consumption was tested with an MSM586SEG (board V1.1).

**4.1.1. Minimum Power-OFF time:****Warning!**

If the power is switched off, the off period must be a minimum of 10 !seconds All capacitors must be fully discharged before a new power-on is performed.

## 4.2. Boot Time

### Test environment for the boot time measurement:

#### Peripherals:

Hard disk Hitachi Mod-DK23AA-60  
 Monitor Compaq Mod-460  
 CompactFlash SanDisk 64MB  
 DOC2000 16MB  
 PS/2-KB Logitech Mod-iTouch Keyboard  
 PS/2-MS Logitech Mod-M-CAA43  
 Floppy TEAC Mod-FD-05HF

#### Software:

MS-DOS V6.22  
 Win98SE Second Edition

### System Boot-Times:

Definitions/Boot-Medium	Normal Boot
MSM586SEG with 64MB SDRAM	time [s]
<b>Boot from floppy disk:</b>	
Boot from Setup Disk1, MS-DOS v6.22 to "Starting MS-DOS" prompt	13
Boot from Setup Disk1, MS-DOS v6.22 to "Welcome to Setup" prompt	35
Boot from "(Sys a:)-Disk" to "A:/>"-Prompt	20
<b>Boot from hard disk-Hitachi Mod-DK23AA-60:</b>	
Boot from hard disk to "Win98SE: Windows notification" prompt	48
<b>Boot from CompactFlash ONT-0515-0006 64MB:</b>	
Boot from CF to "Starting MS-DOS" prompt	13
Boot from CF to "C:\> prompt.	27
<b>Boot from DOC2000 16MB-BIOS: DOC BASE 0 D0000h:</b>	
Boot from DOC2000 to WinCE desktop	Not available at the moment

Boot times are tested with an MSM586SEG (board V1.1).

## 4.3. CPU, Boards and RAMs

### 4.3.1. CPUs of this MICROSPACE Product

Processor	Type	Clock
ELAN520	AMD	133MHz

### 4.3.2. Numeric Coprocessor

The numeric coprocessor is integrated into the ELAN520.

### 4.3.3. DRAM Memory

<b>Speed</b>	70ns
<b>Size</b>	SDRAM SODIMM144
<b>Bits</b>	32bit
<b>Capacity</b>	up to 128MByte
<b>Bank</b>	1-4



#### **Attention!**

Special 32bit wide SODIMM memory is needed.

<b>DLAG Part No.</b>	<b>Size</b>
890655	32MB
890654	64MB
890656	128MB

## 4.4. Interfaces

### 4.4.1. AT Compatible Keyboard & PS/2 Mouse X31

<b>Pin</b>	<b>Signal</b>
1	Speaker out
2	GND
3	External reset input
4	VCC
5	Keyboard Data
6	Keyboard Clock
7	GND
8	External battery 3.0-3.6V
9	Mouse Clock (PS/2)
10	Mouse Data (PS/2)

### 4.4.2. Line Printer Port LPT1

A standard bi-directional LPT port is integrated into the MICROSPACE PC.

Further information about these signals is available in numerous publications, including the IBM technical reference manuals for the PC and AT computers and from other reference documents.

The current is: IOH = 12mA IOL = 24mA

The SUPER I/O 37B787 may be programmed via software commands.

### 4.4.3. Serial Ports COM1-COM2

The serial channels are fully compatible with 16C550 UARTS. COM1 is the primary serial port and is supported by the board's ROM-BIOS as the PC-DOS 'COM1' device. The secondary serial port is COM2; it is supported as the 'COM2' device.

Standard: COM 1/2: National PC87317VUL: 2 x 16C550 compatible serial interfaces  
 COM 3/4: 37B787: 2 x 16C550 compatible serial interfaces

#### Serial Port Connectors COM1, COM2, COM3, COM4:

Pin	Signal Name	Function	in/out	DB25 Pin	DB9 Pin
1	CD	Data Carrier Detect	in	8	1
2	DSR	Data Set Ready	in	6	6
3	RXD	Receive Data	in	3	2
4	RTS	Request To Send	out	4	7
5	TXD	Transmit Data	out	2	3
6	CTS	Clear to Send	in	5	8
7	DTR	Data Terminal Ready	out	20	4
8	RI	Ring Indicator	in	22	9
9	GND	Signal Ground		7	5

The serial port signals are compatible with the RS232C specifications.

### 4.4.4. RS-485

On all MSM586 products, the four serial ports can be ordered with an optional RS-485 interface. Integrated is a one-wire, differential serial interface meeting EIA RS-485 standard specifications. The LTC485 device is used as a UART to RS485 interface transceiver.

The LTC485 is a low power, differential bus/line transceiver designed for multipoint data transmission standard RS485 applications with extended common-mode range 12V to -7V. It also meets the requirements of RS422.

The driver and receiver features three-state outputs, with driver outputs maintaining high impedance over the entire common-mode range. The receiver has a fail-safe feature which guarantees a high output state when the inputs are left open.

The picture below shows a typical application for the RS-485:

**Fehler! Es ist nicht möglich, durch die Bearbeitung von Feldfunktionen Objekte zu erstellen.**

Because the LTC485 has a single differential interface, the receiver and transmitter line signals are looped internally (feedback). For reflexion reasons, the bus must be terminated with 100Ohm on each side.

On the MSM586 boards, the receiver enable input is controlled by the DSR signal from the UART.

The transmitter enable input pin DE is controlled by the CTS signal from the UART.

The LTC485 is a true buffer device, which means, when you write a logical "1" to the send register of the UART, you will see a TTL high state on the TX output pin and the DI input pin of the LTC485.

#### 4.4.4.1. Signal Table

Signal Name	Function
RO	Data output (receiving)
DI	Data input (transmitting)
DE	Transmitter enable
RE#	Receiver inhibit

#### 4.4.4.2. LTC485 Transmitting

Inputs			Line Condition	Outputs	
RE# = DSR	DE = CTS	DI = TXD		B	A
X	1	1	Transmitting	0	1
X	1	0	Transmitting	1	0
X	0	X	High Impedance	Z	Z
X	1	X	Fault	Z	Z

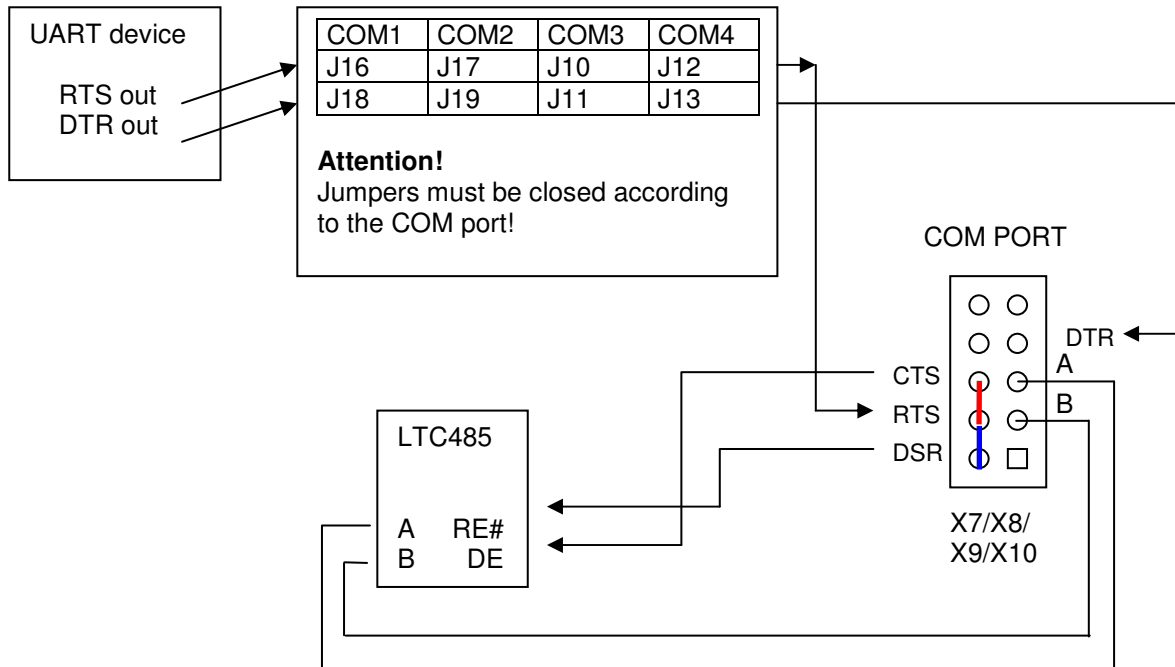
#### 4.4.4.3. LTC485 Receiving

Inputs			Outputs
RE# = DSR	DE = CTS	DI = TXD	RO = RxD
0	0	$\geq 0.2V$	1
0	0	$\leq -0.2V$	0
0	0	Input open	1
1	0	X	Z

#### 4.4.4.4. Enable Signal Controlling

There are different versions of protocols using different UART control signals for switching the receiver and transmitter enable signals RE and DE of the LTC485. The control signal can be selected by an external cable shortcut at the serial interface connector.

The table below describes how to select the control signal:



The Receiver enable signal can be jumpered from DSR-RTS or DSR-DTR.

The Transmitter enable signal can be jumpered from CTS-RTS or CTS-DTR.

This combination is for independent controlling of the receiving/transmitting buffers.

For most applications, a switch to both enable signals is required with the RTS signal by connecting RTS with CTS and DSR together (bridged connection)

#### 4.4.4.5. Software Controlling

For handshaking and switching between transmitting and receiving, a special software protocol is required. There is hardly any software available for supporting one-wire handshaking. Programs like Laplink or Therm95 normally do not support it.

The protocol can be implemented as shown in the following example:

1. The device, which will send a package, must listen to the bus interface.
2. If there is a timeout for approx. 1ms at 9600 baud, device change enables signal RTS from receiving to transmitting.
3. The device sends a synchronising sequence like 00 AA AA AA AA AA 55 to trigger the other peers.
4. The device owns the bus and can send the data package.
5. After sending has finished, the device goes back to receiving modus.

### 4.4.5. Speaker Interface

One of the board's CPU devices provides the logic for a PC compatible speaker port. The speaker logic signal is buffered by a transistor amplifier, and provides approximately 0.1Watt of audio power to an external 8 Ohm speaker. Connect the speaker between VCC and speaker output to have no quiescent current.

### 4.4.6. Floppy Disk Interface

The onboard floppy disk controller and ROM-BIOS support **one** floppy disk drive in any of the standard PC-DOS and MS-DOS formats shown in the table.

#### Supported Floppy Formats:

Capacity	Drive Size	Tracks	Data Rate	DOS Version
1.2MB	5-1/4"	80	500KHz	3.0 - 6.22
720K	3-1/2"	80	250KHz	3.2 - 6.22
1.44M	3-1/2"	80	500KHz	3.3 - 6.22

#### Floppy Interface Configuration

The desired configuration of the floppy drive (number and type) must be properly initialized in the board's CMOS-configuration memory. This is generally done by using "CTRL / ALT / S" at boot up time.

#### Floppy Interface Connector

The table shows the pin-out and signal definitions of the board's floppy disk interface connector. The 26pin high density (1mm pitch FCC) connector has only one drive and motor select. The onboard jumper defines the drive A: or B:. Default is always A:.

#### Floppy Disk Interface Technology

Only CMOS drives are supported. This means the termination resistors are 1 KOhm and 5 1/4"-drives are not recommended (TTL interface).

The 26pin connector: FFC/FPC 0.3mm thick 1.0mm (0.039") pitch (MOLEX 52030 Series)

#### Floppy Disk Interface Connector:

FD26: Pin	Signal Name	Function	in/out
1	VCC	+5Volt	
2	IDX	Index Pulse	in
3	VCC	+5Volt	
4	DS2	Drive Select 2	out
5	VCC	+5Volt	
6	DCHG	Disk Change	in
10	M02	Motor On 2	out
12	DIRC	Direction Select	out
14	STEP	Step	out
16	WD	Write Data	out
17	GND	Signal grounds	
18	WE	Write Enable	out
19	GND	Signal grounds	
20	TRKO	Track 0	in
21	GND	Signal grounds	
22	WP	Write Protect	in
23	GND	Signal grounds	
24	RDD	Read Data	in
25	GND	Signal grounds	
26	HS	Head Select	out

### 4.4.7. LAN Interface

The LAN interface can be enabled or disabled by J31.

If J31 is closed the LAN chip device will be fully isolated from the PCI BUS and not visible by the system BIOS.

The master slot signal pair REQ#/GNT# can now be used for other PCI devices plugged into the PC104+ BUS.

#### LAN Interface Overview

	82559	82559ER	82551QM	82551ER
<b>Product Features</b>				
Data Rates (Mb/s)	10/100	10/100	10/100	10/100
I/O Interface	32-bit PCI	32-bit PCI	32-bit PCI	32-bit PCI
Bus Frequency	33Mhz	33Mhz	33Mhz	33Mhz
Package (dimensions)	15x15mm	15x15mm	15x15mm	15x15mm
Pin Count	196 pin TBGA	196 pin TBGA	196 pin TBGA	196 pin TBGA
TCP, UDP, IPv4 Checksum Offload	Yes	-	Yes	Yes
Wired for Management support	Yes	-	Yes	-
PXE support	Yes	3rd party only	Yes	3rd party only
Alert on LAN 2	Yes	-	-	-
ASF (Tx and Rx alerting)	-	-	Yes	-
SMBus interface	Yes	-	Yes	-
Wake on LAN	Yes	-	Yes	-
Magic Packet	Yes	-	Yes	-
Remote power up support	Yes	-	Yes	-
32-bit PCI/CardBus interface	Yes	-	Yes	-
Modem Interface	Yes	-	Yes	-
VLAN support	Yes	-	Yes	-
Device ID	1229	1209	1229	1209
Available in Ext. Temp (-25-85C)	-	Yes	-	TBD

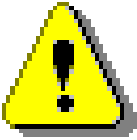
	82559	82559ER	82551QM	82551ER
<b>Software/Driver Support</b>				
ANS support (link aggregation, failover)	Yes	-	Yes	-
NDIS 3, 4	Yes	Yes	Yes	Yes
WinCE 2.12	Yes	Yes	Yes	-
WinCE 3.0	Yes	Yes	Yes	Yes
WinCE 4.0	Yes	Yes	Yes	Yes
Linux	Yes	-	Yes	Yes
Solaris	Yes	-	Yes	-
Netware	Yes	-	Yes	-
SCO OpenServer	Yes	-	Yes	-
FreeBSD	Yes*	Yes*	Yes*	TBD*
NetBSD	Yes*	Yes*	Yes*	TBD*
VxWorks	Yes*	Yes*	Yes*	Yes*
BSD/OS	-	-	TBD*	TBD*
pSOS	Yes*	Yes*	-	-
QNX	Yes*	Yes*	TBD*	TBD*
*through 3rd party ISV				

### 4.4.7.1. Boot from LAN

If you want to boot from LAN, you must enable this function in the BIOS setup:

Enter the BIOS with "CTRL ALT S", set the position "LAN BOOT" in the startup menu to "enable".

For more information, please go to <http://www.etherboot.com/>.



#### **Attention!**

You must install the 32k ATI VGA BIOS otherwise the "LAN BOOT" function will not work.

VGA BIOS	Size	LAN BOOT (32k)	
		Possible	Not possible
M1_DVI.bin	64k		X
M1_TV.bin	64k		X
ATIM132K.bin	32k	X	

(Total ROM size = 64k)

The BIOS is located on the Product CD or in the download area of the support center:

...\products\msm\cpu boards\msm586\_download\MSM586S\_\SEG\VGA\...

Refer to chapter 5.6.2 for downloading the BIOS.

## 4.5. Controllers

### 4.5.1. Interrupt Controllers

An 8259A compatible interrupt controller, within the ELAN520 chipset, provides seven prioritized interrupt levels. Some of these IRQs are normally associated with the board's onboard device interfaces and controllers, and several are available on the AT expansion bus.

Interrupt	PIRQ	Sources	Onboard use
IRQ0		ROM-BIOS clock tick function, from timer 0	yes
IRQ1	PIRQ1	Keyboard controller output buffer full	yes
IRQ2		Used for cascade 2. 8259	yes
IRQ3	PIRQ3	COM2 serial port (COM C or COM D)	yes
IRQ4	PIRQ4	COM1 serial port (COM C or COM D)	yes
IRQ5	PIRQ5	Free for user (COM C or COM D)	(yes) *
IRQ6	PIRQ6	Floppy controller	yes
IRQ7	PIRQ7	LPT1 parallel printer (COM C or COM D)	yes *
IRQ8	PIRQ8	Battery backed clock	yes
IRQ9	PIRQ9	Free for user	no
IRQ10	PIRQ10	<b>Hard disk IDE</b>	yes *
IRQ11	PIRQ0	Free for user	no *
IRQ12	PIRQ2	PS/2 mouse	yes
IRQ13		Math. coprocessor	yes
IRQ14	PIRQ10	Hard disk IDE	yes
IRQ15	PIRQ8	Free for user ( <b>HIGH ACTIVE</b> )	no

\* Depends on the BIOS settings configuration

## 4.6. Timers and Counters

### 4.6.1. Programmable Timers

An 8253 compatible timer/counter device is also included in the board's ASIC device. This device is utilized in precisely the same manner as in a standard AT implementation. Each channel of the 8253 is driven by a 1.190MHz clock, derived from a 14.318MHz oscillator, which can be internally divided in order to provide a variety of frequencies.

Timer 2 can also be used as a general purpose timer if the speaker function is not required.

#### Timer Assignment:

Timer	Function
0	ROM-BIOS clock tick (18.2Hz)
1	DRAM refresh request timing (15 $\mu$ s)
2	Speaker tone generation time base

### 4.6.2. RTC (Real Time Clock)

An AT compatible date/time clock is located within the chipset. The device also contains a CMOS static RAM, compatible with that in standard ATs. System configuration data is normally stored in the clock chip's CMOS RAM in a manner consistent with the convention used in other AT compatible computers.

### 4.6.3. Watchdog

- The watchdog function is an implemented function of the ELAN520 and must be set/triggered by the application.
- The watchdog is hardware triggered and will also be activated in case the system hangs.
- The watchdog is programmable between 0.5ms and 32sec.
- The RESWDOG.CCP is a programming sample of how to implement it into the customer's application. Any comments/explanations are integrated inside the file.
- There are no hardware modifications necessary on the delivered and future boards to support the watchdog function. This will be the standard watchdog function on all our MSM586Sxx.

**RESWDOG**

```
#include <stdio.h>
#include <conio.h>
#include <dos.h>

void main()
{
    unsigned char kk;
    unsigned int tt = 0x10; //timeout = 4 Sec.
    //TIMEOUT values:
    // tt = 0 - invalid value
    // tt = 0x01 - 0.5 uSec
    // tt = 0x02 - 0.5 mSec
    // tt = 0x04 - 1.0 Sec
    // tt = 0x08 - 2.0 Sec
    // tt = 0x10 - 4.0 Sec
    // tt = 0x20 - 8.0 Sec
    // tt = 0x40 - 16.0 Sec
    // tt = 0x80 - 32.0 Sec

    //pointer to address of WATCHDOG Timer Control
    unsigned int far *ff = (unsigned int far*)MK_FP(0xE000,0xFCB0); //E000:FCB0

    printf("Press ESC to quit\n");
    //initialization sequence, enable WATCHDOG and assign the timeout (tt)
    *ff = 0x3333;
    *ff = 0xCCCC;
    *ff = 0xC000 | tt;

    //program body - user code
    while(1)
    {
        if(kbhit())
        {
            if(getch() == 0x1B) return; //return to OS. In this sample,
            //PC will reboot after 4 Sec.
        }
        printf("%02X\r",kk++); //nothing, just to do something
        //.....
        //"magic" sequence, for cleaning WATCHDOG counter
        //the timing interval between such sequences must be
        //not less than watchdog timeout(for this sample < 4 Sec)
        *ff = 0xAAAA;
        *ff = 0x5555;
    }
}
```

## 4.7. Remote Function

Remote works only with the **COM 1** port on the MSM586SEG.

**BIOS default settings are normally as follows:**

<b>Internal ELAN A</b>	<b>J4</b>	<b>COM 1</b>
Internal ELAN B	J41	NONE
SUPER I/O C	J50	NONE
SUPER I/O D	J49	COM 2

**More details are available in the separate BIOS manual on the Product CD and on our homepage.**

### 4.7.1. Remote Features

FS FORTH-SYSTEME has added its remote package "Embedded Support Kit" to the AMD ÉlanSC520 BIOS. The Embedded Support Kit allows you to control your target machine from a host computer using either a serial or parallel null-modem cable. This is accomplished by transferring all INT10h (video) and INT16h (keyboard) requests to the host machine, executing the command there, and finally returning the results back to the target system. The target system seems to behave just like it would use its own VGA card and keyboard, but in fact it uses the resources of the host computer. Additionally, the target can access the floppy drive and the hard disk of your host PC.

These features are of great value when you bring up your own board for the first time. In embedded systems, typical PC components are often left out to save costs. A standard BIOS typically would stop and warn the user that devices are missing. The BIOS has been modified to go on even if there is no keyboard or display adapter. With the "Embedded Support Kit", users can almost work with such machines as they are used to on a standard PC. The BIOS contains support for both serial and parallel transmission.

#### 4.7.1.1. The Remote Server REMHOST.EXE

The utility REMHOST is started on the host computer. It listens on the serial or parallel port for incoming target requests, executes the commands and sends the output values back.

The user can decide on the host machine, in a configuration file, which devices the target system should redirect. By default, the target assumes to redirect video and keyboard services.

The following options are available in the configuration file REMHOST.INI:

```

PORT=1           // COM or LPT port number
LPT *           // use parallel port for transmission
                // comment this for serial port
FLOPPY          // enable host floppy
FLOPPY=ROMDISK.IMG // use a floppy disk image
WRPROT          // simulate write-protection for remote drives
NOKEYB          // disable host keyboard
NOVIDEO         // disable host video
DUALVIDEO       // use target display and remote video simultaneously

```

Within the configuration file, you can add comments with "/\*". Instead of using a real floppy drive, you can also generate image files of floppy disks. Access to these image files are much faster than to real floppy disks. Additionally, the image files can be write-protected. So you can build up virtual floppy drives to initially set up the target's file system or to start test tools during production.

Floppy disk images can be produced with the utility FDIMAGE. Type "FDIMAGE /H" to get a list of available options.

**Rem:** \* not supported, needs a customized BIOS

When video redirection is enabled (option "NOVIDEO" is *not* active), the BIOS will skip the initialization of both ISA and PCI VGA cards. The BIOS thereby comes up much quicker. Using the keyword DUALVIDEO will enable possible VGA cards as well and display video output on both the real video card and on the remote machine. This allows hardware engineers to debug VGA controller problems.

As soon as remote keyboard is enabled, the BIOS will not warn when keyboards are missing.

You can leave REMHOST by pressing the left SHIFT and STRG keys simultaneously.

#### 4.7.1.2. Remote Enabler

To enable the remote function, one must make a hardware switch as follows:

- Pin 4 (DTR) and Pin 9 (RI) must be bridged on the target PC.
- Leave Pin 9 unconnected (open) from the host PC.

#### 4.7.1.3. Cable Definition (DSUB-9pin-female)

The wiring of the **serial null-modem cable** is as follows:

PC1 (Host)			PC2 (Target)	
Signal Name	DSUB-Pin Number		DSUB-Pin Number	Signal Name
DCD	1	--	7, 8	RTS, CTS
RxD	2	--	3	TxD
TxD	3	--	2	RxD
DTR	4	--	6	DSR
GND	5	--	5	GND
DSR	6	--	4	DTR
RTS, CTS	7, 8	--	1	DCD

#### Optional:

The wiring of the **parallel DOS/Link-Cable** (DSUB 25pin) is as follows:

PC1 (Host)			PC2 (Target)	
Signal Name	DSUB-Pin Number		DSUB-Pin Number	Signal Name
D0	2	--	15	ERROR#
D1	3	--	13	SLCT
D2	4	--	12	PE
D3	5	--	10	ACK#
D4	6	--1	1	BUSY
ERROR#	15	--	2	D0
SLCT	13	--	3	D1
PE	12	--	4	D2
ACK#	10	--	5	D3
BUSY	11	--	6	D4
AFDT#	14	--	14	AFDT#
INIT#	16	--	16	NIT#
SLCTIN#	17	--	17	SLCTIN#
STROBE#	1	--	1	STROBE#
GND	25	--	25	GND

#### 4.7.1.4. Restrictions

When using the ESC or writing programs that should also work with redirection, please keep the following restrictions in mind:

- WindowsNT denies direct access to hardware I/O ports. If you plan to use REMHOST in a WindowsNT environment, an additional software package is required that gives access to the specific I/O ports. This software package is available from FS FORTH-SYSTEME.
- Avoid direct writes to video RAM; there is no mechanism to detect and transfer these outputs.
- Since DOS7 of Windows95, standard console output is partially written to the video screen. So you will only see some characters displayed on the host machine while the rest are displayed on the target's video display.
- Avoid video calls that use registers other than AX, BX, CX and DX. To speed up video output, only these registers will be transferred. The other registers will be typically used as pointers to data buffers.
- Formatting of remote floppy is not supported.
- Don't rely on "Keyboard Intercept" INT15/4F. This function is no longer available.
- KEYB.COM is no longer needed on the target machine. Instead, the current keyboard handler of your host computer is automatically used.
- Don't press "Ctrl Alt Del" while redirection is active. This will **not** reboot your target system, but **will** reboot your host machine!

## 4.8. BIOS

### 4.8.1. BIOS History

Version	Date	Status	Modifications
V1.26	08.2003	Released	

## 4.8.2. Core BIOS download

### 4.8.2.1. Before downloading a BIOS

Please read through this section carefully and prepare for the download.

#### **Make an MSDOS 6.22 bootable diskette which includes the following files:**

DELEP520.EXE  
Flash520.exe  
core BIOS (M520xxx.cor)  
lcd\_file.000



#### ***Important...***

Do not use boot disks created in a Windows operating system. If you do not have an MSDOS 6.22 disk available, you can download a boot disk from [www.bootdisk.com](http://www.bootdisk.com).

### 4.8.2.2. CORE BIOS download function

- Select the SHADOW option in the BIOS, for a BIOS and VGA (if this option is available).
- Disable the EMM386 or other memory managers in the CONFIG.SYS of your boot disk.
- Make sure that the Flash520.EXE program and the BIOS to download are on the same path and directory!
- Boot the DOS without config.sys and autoexec.bat → press **F5** while starting the DOS boot.
- Check where the download tool is located, that the available disk space is larger than 64kB (for safe storage).
- Make sure the floppy disk is not write-protected.

### 4.8.2.3. Start the downloading process

1. Start the system with the bootable diskette. If you do not have a bootable diskette or floppy drive, you can start in DOS mode by pressing the **F5** key to disable autoexec.bat and config.sys.
2. Run DELEP520.EXE to clear the CMOS and the EEPROM.



#### ***Important...***

***If you do not run DELEP520.EXE, the system will be destroyed during the BIOS upgrade!***

3. Run Flash520.EXE M520xxx.cor
4. When the BIOS download is finished, power-off the system.
5. After powering the system back on, press **Ctrl ALT S** to enter setup. Set the default values and then exit the setup with "save and reboot".
6. Switch off the system. The download procedure is now finished.

### 4.8.2.4. If the download does not work:

- Check if the EMM386 is not loaded.
- Check if there is a peripheral card in the system which would occupy the same memory range. If one is present, disconnect it.
- If the download stopped or did not finish, make a warm boot\* and repeat the steps or download another file. (\* As the video is shadowed, everything is visible and a cold boot would clear the screen so nothing would be visible afterwards.)

### 4.8.3. ROM-BIOS Sockets

An EPROM socket with 8bit wide data access normally contains the board's AT compatible ROM-BIOS. The socket takes a 29F40 EPROM (or equivalent) device. The board's wait-state control logic automatically inserts four memory wait states in all CPU accesses to this socket.

The ROM-BIOS sockets occupy the memory area from C0000H through FFFFFh; however, the board's ASIC logic reserves the entire area from C0000h through FFFFFh for onboard devices, so that this area is already usable for ROM-DOS and BIOS expansion modules. Consult the appropriate address map for the MICROSPACE MSM586SEV ROM-BIOS sockets.

#### 4.8.3.1. Standard BIOS ROM

<b>Core BIOS Device</b>	29F040	(U111) socket
<b>VGA BIOS Device</b>	29F010	(U155) soldered
<b>Map</b>	E0000 - FFFFFh	BIOS from INSYDE SOFT 128k
	C0000 - CFFFFh	VGA BIOS from ATI Technology 64k

### 4.8.4. BIOS Data Area Definitions

The BIOS Data Area is an area within system RAM that contains information about the system environment. System environment information includes definitions associated with hard disks, diskette drives, keyboard, video, as well as other BIOS functions. This area is created when the system is first powered on. It occupies a 256Byte area from 0400h - 04FFh. The following table lists the contents of the BIOS Data Area locations in offset order starting from segment address 40:00h.

BIOS Data Area Definitions	
Location	Description
00h - 07h	I/O addresses for up to 4 serial ports
08h - 0Dh	I/O addresses for up to 3 parallel ports
0Eh - 0Fh	Segment address of extended data address
10h - 11h	Equipment list bits 15-14 = Number of parallel printer adapters 00 = Not installed 01 = One 10 = Two 11 = Three bits 13-12 = Reserved bits 11-9 = Number of serial adapters 00 = Not installed 001 = One 010 = Two 011 = Three 100 = Four bit 8 = Reserved bits 7-6 = Number of diskette drives 00 = One drive 01 = Two drives bits 5-4 = Initial video mode 00 = EGA or VGA 01 = 40 x 25 color 10 = 80 x 25 color 11 = 80 x 25 monochrome bit 3 = Reserved bit 2 = (1) Pointing device present bit 1 = (1) Math coprocessor present bit 0 = (1) Diskette drive present
12h	Reserved for port testing by manufacturer bits 7-1 = Reserved bit 0 = (0) Non-test mode (1) Test mode
13h	Memory size in kiloBytes - low Byte
14h	Memory size in kiloBytes - high Byte
15h - 16h	Reserved
17h	Keyboard Shift Qualifier States bit 7 = Insert mode bit 6 = CAPS lock bit 5 = Numlock bit 4 = Scroll Lock bit 3 = Either Alt key bit 2 = Either Control key bit 1 = Left Shift key bit 0 = Right Shift key 0 = not set    1 = set
18h	Keyboard Toggle Key States bit 7 = (1) Insert held down bit 6 = (1) CAPS lock held down bit 5 = (1) Num Lock held down bit 4 = (1) Scroll Lock held down bit 3 = (1) Control+Num Lock held down bit 2 = (1) Sys Re held down bit 1 = (1) Left Alt held down bit 0 = (1) Left Control held down
19h	Scratch area for input from Alt key and numeric keypad
1Ah - 1Bh	Pointer to next character in keyboard buffer
1Ch - 1Dh	Pointer to last character in keyboard buffer

BIOS Data Area Definitions	
Location	Description
1Eh - 3Dh	Keyboard Buffer. Consists of 16 word entries.
3Eh	Diskette Drive Recalibration Flag bit 7 = (1) Diskette hardware interrupt occurred bits 6-4 = Not used bits 3-2 = Reserved bit 1 = (0) Recalibrate drive B bit 0 = (0) Recalibrate drive A
3Fh	Diskette Drive Motor Status bit 7 = Current operation 0 = Write or Format 1 = Read or Verify bit 6 = Reserved bits 5-4 = Drive Select 00 = Drive A 01 = Drive B bits 3-2 = Reserved 0 = Disable 1 = Enabled bit 1 = Drive B Motor Status 0 = Off 1 = On bit 1 = Drive A Motor Status 0 = Off 1 = On
40h	Diskette Drive Motor Timeout Disk drive motor is powered off when the value via the INT 08h timer interrupt reaches 0.
41h	Diskette Drive Status bit 7 = Drive Ready 0 = Ready 1 = Not ready bit 6 = Seek Error 0 = No error 1 = Error occurred bit 5 = Controller operation 0 = Working 1 = Failed bits 4-0 = Error Codes 00h = No error 01h = Invalid function requested 02h = Address mark not located 03h = Write protect error 04h = Sector not found 06h = Diskette change line active (door opened) 08h = DMA overrun error 09h = Data boundary error 0Ch = Unknown media type 10h = ECC or CRC error 20h = Controller failure 40h = Seek operation failure 80h = Timeout
42h - 48h	Diskette Controller Status Bytes
49h	Video Mode Setting
4Ah - 4Bh	Number of Columns on screen
4Ch - 4Dh	Size of Current Page, in Bytes
4Eh - 4Fh	Address of Current Page
50h - 5Fh	Position of cursor for each video page. Current cursor position is stored two Bytes per page. First Byte specifies the column, the second Byte specifies the row.

BIOS Data Area Definitions	
Location	Description
60h - 61h	Start and end lines for 6845-compatible cursor type. 60h = starting scan line 61h = ending scan line
62h	Current Video Display Page
63h - 64h	6845-compatible I/O port address for current mode 3B4h = Monochrome 3D4h = Color
65h	Register for current mode select
66h	Current palette setting
67 - 6Ah	Address of adapter ROM
6Bh	Last interrupt that occurred
6Ch - 6Dh	Low word of timer count
6Eh - 6Fh	High word of timer count
70h	Timer count for 24-hour rollover flag
71h	Break key flag
72h - 73h	Reset flag 1243h = Soft reset. Memory test is bypassed.
74h	Status of last hard disk operation 00h = No error 01h = Invalid function requested 02h = Address mark not located 03h = Write protect error 04h = Sector not found 05h = Reset failed 08h = DMA overrun error 09h = Data boundary error 0Ah = Bad sector flag selected 0Bh = Bad track detected 0Dh = Invalid number of sectors on format 0Eh = Control data address mark detected 0Fh = DMA arbitration level out of range 10h = ECC or CRC error 11h = Data error corrected by ECC 20h = Controller failure 40h = Seek operation failure 80h = Timeout AAh = Drive not ready BBh = Undefined error occurred CCh = Write fault on selected drive E0h = Status error or error register = 0 FFh = Sense operation failed
75h	Number of hard drives
76h - 77h	Work area for hard disk
78h - 7Bh	Default parallel port timeout values
7Dh - 7Fh	Default serial port timeout values
80h - 81h	Pointer to start of keyboard buffer
82h - 83h	Pointer to end of keyboard buffer
84h - 88h	Reserved for EGA/VGA BIOS
8Ah	Reserved

BIOS Data Area Definitions	
Location	Description
8Bh	Diskette drive data transfer rate information bits 7-5 = Data rate on last operation 00 = 500 KBS 01 = 300 KBS 10 = 250 KBS bits 5-4 = Last drive step rate selected bits 3-2 = Data transfer rate at start of operation 00 = 500 KBS 01 = 300 KBS 10 = 250 KBS bits 1-0 = Reserved
8Ch	Copy of hard status register
8Dh	Copy of hard drive error register
8Eh	Hard drive interrupt flag
8Fh	Diskette controller information bit 7 = Reserved bit 6 = (1) Drive confirmed for drive B bit 5 = (1) Drive B is multi-rate bit 4 = (1) Drive B supports line change bit 3 = Reserved bit 2 = (1) Drive determined for drive A bit 1 = (1) Drive B is multi-rate bit 0 = (1) Drive B supports line change
90h - 91h	Media type for drives bits 7-6 = Data transfer rate 00 = 500 KBS 01 = 300 KBS 10 = 250 KBS bit 5 = (1) Double stepping required when 360K diskette inserted into 1.2MB drive bit 4 = (1) Known media is in drive bit 3 = Reserved bits 2-0 = Definitions upon return to user applications 000 = Testing 360K in 360K drive 001 = Testing 360K in 1.2 MB drive 010 = Testing 1.2 MB in 1.2 MB drive 011 = Confirmed 360K in 360K drive 100 = Confirmed 360K in 1.2 MB 101 = Confirmed 1.2 MB in 1.2 MB drive 111 = 720K in 720K drive or 1.44 MB in 1.44 MB drive
92h - 93h	Scratch area for diskette media. Low Byte for drive A, high Byte for drive B.
94h - 95h	Current track number for both drives. Low Byte for drive A, high Byte for drive B.
96h	Keyboard Status bit 7 = (1) Read ID bit 6 = (1) Last code was first ID bit 5 = (1) Force to Num Lock after read ID bit 4 = (1) Enhanced keyboard installed bit 3 = (1) Right ALT key active bit 2 = (1) Right Control key active bit 1 = (1) Last code was E0h bit 0 = (1) Last code was E1h
97h	Keyboard Status bit 7 = (1) Keyboard error bit 6 = (1) Updating LEDs bit 5 = (1) Resend code received bit 4 = (1) Acknowledge received bit 3 = Reserved bit 2 = (1) Caps lock LED state bit 1 = (1) Num lock LED state bit 0 = (1) Scroll lock LED state

BIOS Data Area Definitions	
Location	Description
98h - 99h	Offset address of user wait flag
9Ah - 9Bh	Segment address of user wait flag
9Ch - 9Dh	Wait count, in microseconds (low word)
9Eh - 9Fh	Wait count, in microseconds (high word)
A0h	Wait active flag bit 7 = (1) Time has elapsed bits 6-1 = Reserved bit 0 = (1) INT 15h, AH = 86h occurred
A1h - A7h	Reserved
A8h - ABh	Pointer to video parameters and overrides
ACh - FFh	Reserved
100h	Print screen status Byte

#### 4.8.5. Compatibility Service Table

In order to ensure compatibility with industry-standard memory locations for interrupt service routines and miscellaneous tabular data, the BIOS maintains tables and jump vectors.

Location	Description
FE05Bh	Entry Point for POST
FE2C3h	Entry point for INT 02h (NMI service routine)
FE3FEh	Entry point for INT 13h (Diskette Drive Services)
FE401h	Hard Drive Parameters Table
FE6F1h	Entry point for INT 19h (Bootstrap Loader routine)
FE6F5h	System Configuration Table
FE739h	Entry point for INT 14h (Serial Communications)
FE82Eh	Entry point for INT 16h (Keyboard Services)
FE897h	Entry point for INT 09h (Keyboard Services)
FEC59h	Entry point for INT 13h (Diskette Drive Services)
FEF57h	Entry point for INT 0Eh (Diskette Hardware Interrupt)
FEFC7h	Diskette Drive Parameters Table
FEFD2h	Entry point for INT 17h (Parallel Printer Services)
FF065h	Entry point for INT 10h (CGA Video Services)
FF0A4h	Video Parameter Table (6845 Data Table - CGA)
FF841h	Entry point for INT 12h (Memory Size Service)
FF84Dh	Entry point for INT 11h (Equipment List Service)
FF859h	Entry point for INT 15h (System Services)
FFA6Eh	Video graphics and text mode tables
FFE6Eh	Entry point for INT 1Ah (Time-of-Day Service)
FFEA5h	Entry Point for INT 08h (System Timer Service)
FFEF3h	Vector offset table loaded by POST
FFF53h	Dummy Interrupt routine IRET Instruction
FFF54h	Entry point for INT 05h (Print Screen Service)
FFFF0h	Entry point for Power-on
FFFF5h	BIOS Build Date (in ASCII)
FFFFEh	BIOS ID

## 4.9. CMOS RAM Map

Systems based on the industry-standard specification include a battery backed Real Time Clock chip. This clock contains at least 64Bytes of non-volatile RAM. The system BIOS uses this area to store information including system configuration and initialization parameters, system diagnostics, and the time and date. This information remains intact even when the system is powered down.

The BIOS supports 128Bytes of CMOS RAM. This information is accessible through I/O ports 70h and 71h. CMOS RAM can be divided into several segments:

- Locations 00h - 0Fh contain the real time clock (RTC) and status information
- Locations 10h - 2Fh contain system configuration data
- Locations 30h - 3Fh contain system BIOS-specific configuration data as well as chipset-specific information
- Locations 40h - 7Fh contain chipset-specific information as well as power management configuration parameters

The following table provides a summary of how these areas may be further divided.

Beginning	Ending	Checksum	Description
00h	0Fh	No	RTC and Checksum
10h	2Dh	Yes	System Configuration
2Eh	2Fh	No	Checksum Value of 10h - 2Dh
30h	33h	No	Standard CMOS
34h	3Fh	No	Standard CMOS - SystemSoft Reserved
40h	5Bh	Yes	Extended CMOS - Chipset Specific
5Ch	5Dh	No	Checksum Value of 40h - 5Bh
5Eh	6Eh	No	Extended CMOS - Chipset Specific
6Fh	7Dh	Yes	Extended CMOS - Power Management
7Eh	7Fh	No	Checksum Value of 6Fh - 7Dh

CMOS Map	
Location	Description
00h	Time of day (seconds) specified in BCD
01h	Alarm (seconds) specified in BCD
02h	Time of day (minutes) specified in BCD
03h	Alarm (minutes) specified in BCD
04h	Time of day (hours) specified in BCD
05h	Alarm (hours) specified in BCD
06h	Day of week specified in BCD
07h	Day of month specified in BCD
08h	Month specified in BCD
09h	Year specified in BCD
0Ah	Status Register A bit 7 = Update in progress bits 6-4 = Time based frequency divider bits 3-0 = Rate selection bits that define the periodic interrupt rate and output frequency.
0Bh	Status Register B bit 7 = Run/Halt 0 Run 1 Halt bit 6 = Periodic Timer 0 Disable 1 Enable bit 5 = Alarm Interrupt 0 Disable 1 Enable bit 4 = Update Ended Interrupt 0 Disable 1 Enable bit 3 = Square Wave Interrupt 0 Disable 1 Enable bit 2 = Calendar Format 0 BCD 1 Binary bit 1 = Time Format 0 12-Hour 1 24-Hour bit 0 = Daylight Savings Time 0 Disable 1 Enable
0Ch	Status Register C bit 7 = Interrupt Flag bit 6 = Periodic Interrupt Flag bit 5 = Alarm Interrupt Flag bit 4 = Update Interrupt Flag bits 3-0 = Reserved
0Dh	Status Register D bit 7 = Real Time Clock 0 Lost Power 1 Power
0Eh	CMOS Location for Bad CMOS and Checksum Flags bit 7 = Flag for CMOS Lost Power 0 = Power OK 1 = Lost Power bit 6 = Flag for CMOS checksum bad 0 = Checksum is valid 1 = Checksum is bad
0Fh	Shutdown Code

CMOS Map	
Location	Description
10h	Diskette Drives bits 7-4 = Diskette Drive A 0000 = Not installed 0001 = Drive A = 360 kB 0010 = Drive A = 1.2MB 0011 = Drive A = 720 kB 0100 = Drive A = 1.44MB 0101 = Drive A = 2.88MB bits 3-0 = Diskette Drive B 0000 = Not installed 0001 = Drive B = 360 kB 0010 = Drive B = 1.2MB 0011 = Drive B = 720 kB 0100 = Drive B = 1.44MB 0101 = Drive B = 2.88MB
11h	Reserved
12h	Fixed (Hard) Drives bits 7-4 = Hard Drive 0, AT Type 0000 = Not installed 0001-1110 = Types 1-14 1111 = Extended drive types 16-44. See location 19h. bits 3-0 = Hard Drive 1, AT Type 0000 = Not installed 0001-1110 = Types 1-14 1111 = Extended drive types 16-44. See location 2Ah.
13h	Reserved
14h	Equipment bits 7-6 = Number of Diskette Drives 00 = One diskette drive 01 = Two diskette drives 10, 11 = Reserved bits 5-4 = Primary Display Type 00 = Adapter with option ROM 01 = CGA in 40 column mode 10 = CGA in 80 column mode 11 = Monochrome bits 3-2 = Reserved bit 1 = Math Coprocessor Presence 0 = Not installed 1 = Installed bit 0 = Bootable Diskette Drive 0 = Not installed 1 = Installed
15h	Base Memory Size (in kB) - Low Byte
16h	Base Memory Size (in kB) - High Byte
17h	Extended Memory Size (in kB) - Low Byte
18h	Extended Memory Size (in kB) - High Byte
19h	Extended Drive Type - Hard Drive 0
1Ah	Extended Drive Type - Hard Drive 1

CMOS Map	
Location	Description
1Bh	Custom and Fixed (Hard) Drive Flags bits 7-6 = Reserved bit 5 = Internal Floppy Disk Controller 0 = Disabled 1 = Enabled bit 4 = Internal IDE Controller 0 = Disabled 1 = Enabled bit 3 = Hard Drive 0 Custom Flag 0 = Disabled 1 = Enabled bit 2 = Hard Drive 0 IDE Flag 0 = Disabled 1 = Enabled bit 1 = Hard Drive 1 Custom Flag 0 = Disabled 1 = Enabled bit 0 = Hard Drive 1 IDE Flag 0 = Disabled 1 = Enabled
1Ch	Reserved
1Dh	EMS Memory Size Low Byte
1Eh	EMS Memory Size High Byte
1Fh - 24h	Custom Drive Table 0 These 6 Bytes (48 bits) contain the following data: Cylinders                   10bits   range 0-1023 Landing Zone               10bits   range 0-1023 Write Precompensation   10bits   range 0-1023 Heads                       8bits    range 0-15 Sectors/Track             8bits    range 0-254
1Fh	Byte 0 bits 7-0 = Lower 8 bits of Cylinders
20h	Byte 1 bits 7-2 = Lower 6 bits of Landing Zone bits 1-0 = Upper 2 bits of Cylinders
21h	Byte 2 bits 7-4 = Lower 4 bits of Write Precompensation bits 3-0 = Upper 4 bits of Landing Zone
22h	Byte 3 bits 7-6 = Reserved bits 5-0 = Upper 6 bits of Write Precompensation
23h	Byte 4 bits 7-0 = Number of Heads
24h	Byte 5 bits 7-0 = Sectors Per Track
25h - 2Ah	Custom Drive Table 1 These 6 Bytes (48 bits) contain the following data: Cylinders                   10bits   range 0-1023 Landing Zone               10bits   range 0-1023 Write Precompensation   10bits   range 0-1023 Heads                       8bits    range 0-15 Sectors/Track             8bits    range 0-254
25h	Byte 0 bits 7-0 = Lower 8 bits of Cylinders
26h	Byte 1 bits 7-2 = Lower 6 bits of Landing Zone bits 1-0 = Upper 2 bits of Cylinders

CMOS Map	
Location	Description
27h	Byte 2 bits 7-4 = Lower 4 bits of Write Precompensation bits 3-0 = Upper 4 bits of Landing Zone
28h	Byte 3 bits 7-6 = Reserved bits 5-0 = Upper 6 bits of Write Precompensation
29h	Byte 4 bits 7-0 = Number of Heads
2Ah	Byte 5 bits 7-0 = Sectors Per Track
2Bh	Boot Password bit 7 = Enable/Disable Password 0 = Disable Password 1 = Enable Password bits 6-0 = Calculated Password
2Ch	SCU Password bit 7 = Enable/Disable Password 0 = Disable Password 1 = Enable Password bits 6-0 = Calculated Password
2Dh	Reserved
2Eh	High Byte of Checksum - Locations 10h to 2Dh
2Fh	Low Byte of Checksum - Locations 10h to 2Dh
30h	Extended RAM (kB) detected by POST - Low Byte
31h	Extended RAM (kB) detected by POST - High Byte
32h	BCD Value for Century
33h	Base Memory Installed bit 7 = Flag for Memory Size 0 = 640kB 1 = 512kB bits 6-0 = Reserved
34h	Minor CPU Revision Differentiates CPUs within a CPU type (i.e., 486SX vs 486 DX, vs 486 DX/2). This is crucial for correctly determining CPU input clock frequency. During a power-on reset, Reg DL holds minor CPU revision.
35h	Major CPU Revision Differentiates between different CPUs (i.e., 386, 486, Pentium). This is crucial for correctly determining CPU input clock frequency. During a power-on reset, Reg DH holds major CPU revision.
36h	Hotkey Usage bits 7-6 = Reserved bit 5 = Semaphore for Completed POST bit 4 = Semaphore for 0 Volt POST (not currently used) bit 3 = Semaphore for already in SCU menu bit 2 = Semaphore for already in PM menu bit 1 = Semaphore for SCU menu call pending bit 0 = Semaphore for PM menu call pending
40h-7Fh	Definitions for these locations vary depending on the chipset.

### 4.9.1. BIOS CMOS Setup

If wrong setups are memorized in the CMOS-RAM, the default values will be loaded after resetting the RTC/CMOS-RAM with the CMOS-RESET jumper.

If the battery is down and the EEPROM values are faulty, it is always possible to start the system with the default values from the BIOS.



#### **Attention!**

On the next setup pages (switch with **TAB**), the values for special parameters are modifiable. Normally the parameters are set correctly by DIGITAL-LOGIC AG. **Be very careful in modifying any parameters as the system could crash.**

Some parameters are dependent on the CPU type. For example, the cache parameter is always available. If you select too few wait-states, the system will not start until you reset the CMOS-RAM using the RAM-Reset jumper or unsoldering the battery, but the default values are reloaded. *If you are not familiar with these parameters, do not change anything!*

## 4.10. EEPROM saved CMOS Setup

The EEPROM has different functions, as listed below:

- Backup of the CMOS-Setup values.
- Storing system information like: version, production date, customization of the board, CPU type.
- Storing user/application values.

The EEPROM will **not** be updated automatically after exiting the BIOS setup menu. The system will also operate without any CMOS battery regardless of the CMOS setup values. In this case, the CMOS is automatically updated with the EEPROM values.

To store your defined configuration to the EEPROM, you have to choose "Save to EEPROM" in the menu "Exit".

To get the real default values (factory settings), please use the tool "DEFAULT.EXE" which is located on the Product CD or the download area in the DLAG Support Center.

The user may access the EEPROM through the INT15 special functions. **\*\* Refer to that chapter in the BIOS manual on the Product CD.**

The system information is read-only and uses the SFI functions. **\*\* Refer to the BIOS manual.**

### 4.10.1. EEPROM Memory for Setup

The EEPROM is used for setup and configuration data, stored as an alternative to the CMOS-RTC. Optionally, the EEPROM setup driver may update the CMOS RTC, if the battery is running down and the checksum error would appear and stop the system. The capacity of the EEPROM is 2 kByte.

#### Organization of the 2048Byte EEPROMs:

Address MAP	Function
0000h	CMOS-Setup valid (01=valid)
0001h	Reserved
0003h	Flag for DLAG-Message (FF=no message)
0010h-007Fh	Copy of CMOS-Setup data
0080h-00FFh	Reserved for AUX-CMOS-Setup
0100h-010Fh	Serial-Number
0110h-0113h	Production date (year/day/month)
0114h-0117h	1. Service date (year/day/month)
0118h-011Bh	2. Service date (year/day/month)
011Ch-011Fh	3. Service date (year/day/month)
0120h-0122h	Boot errors (Auto incremented if any boot error occurs)
0123h-0125h	Setup Entries (Auto incremented on every Setup entry)
0126h-0128h	Low Battery (Auto incremented every time the battery is low, EEPROM -> CMOS)
0129h-012Bh	Startup (Auto incremented on every power-on start)
0130h	Reserved
0131h	Reserved
0132h/0133h	BIOS Version (V1.4 => [0132h]:= 4, [0133h]:=1)
0134h/0135h	BOARD Version (V1.5 => [0124h]:=5, [0125h]:=1)
0136h	BOARD TYPE ('M'=PC/104, 'E'=Euro, 'W'=MSWS, 'S'=Slot, 'C'=Custom, 'X'= smartCore or smartModule)
0137h	CPU TYPE: (01h=ELAN300/310, 02h=ELAN400, 05h=P5, 08h=P3, 09h=ELAN520, 10h=P-M).
0200h-03FFh	Reserved
0200h-027Fh	Reserved
0400h-07FFh	Free for Customer use

## 4.11. Memory

### 4.11.1. System Memory Map

The ELAN520 CPU, used as central processing unit on the MICROSPACE, has a memory address space which is defined by 32 address bits. Therefore, it can address 1 GByte of memory. The memory address MAP is as follows:

#### CPU

Address	Size	Function / Comments
000000 - 09FFFFh	640 KBytes	Onboard DRAM for DOS applications
0A0000 - 0BFFFFh	128 KBytes	CGA, EGA, LCD Video RAM 128kB
0C0000 - 0CFFFFh	64 KBytes	VGA BIOS, selected by the hardware
0D0000 - 0D4000h	16 KBytes	Free for user
0D4000 - 0D8000h	16 KBytes	Free for user
0D8000 - 0DFFFFh	32 KBytes	Free for user
0E0000 - 0EFFFFh	64 KBytes	BIOS
0F0000 - 0FFFFFFh	64 KBytes	BIOS
100000 - 1FFFFFFh	1 MByte	DRAM for extended onboard memory
200000 - FFFFFFFh	14 MBytes	DRAM for extended onboard memory

\*\* Please also refer to the BIOS manual for further details.

## 4.11.2. System I/O Map

The following table shows the detailed listing of the I/O port assignments used in the MICROSPACE board:

I/O Address	Read/Write Status	Description
0000h	R / W	DMA channel 0 address byte 0 (low), then byte 1
0001h	R / W	DMA channel 0 word count byte 0 (low), then byte 1
0002h	R / W	DMA channel 1 address byte 0 (low), then byte 1
0003h	R / W	DMA channel 1 word count byte 0 (low), then byte 1
0004h	R / W	DMA channel 2 address byte 0 (low), then byte 1
0005h	R / W	DMA channel 2 word count byte 0 (low), then byte 1
0006h	R / W	DMA channel 3 address byte 0 (low), then byte 1
0007h	R / W	DMA channel 3 word count byte 0 (low), then byte 1
0008h	R	DMA channel 0-3 status register bit 7 = 1 Channel 3 request bit 6 = 1 Channel 2 request bit 5 = 1 Channel 1 request bit 4 = 1 Channel 0 request bit 3 = 1 Terminal count on channel 3 bit 2 = 1 Terminal count on channel 2 bit 1 = 1 Terminal count on channel 1 bit 0 = 1 Terminal count on channel 0
0008h	W	DMA channel 0-3 command register bit 7 = DACK sense active high/low 0 low 1 high bit 6 = DREQ sense active high/low 0 low 1 high bit 5 = Write selection 0 Late write selection 1 Extended write selection bit 4 = Priority 0 Fixed 1 Rotating bit 3 = Timing 0 Normal 1 Rotating bit 2 = Controller enable/disable 0 Enable 1 Disable bit 1 = Memory-to-memory enable/disable 0 Disable 1 Enable bit 0 = Reserved
0009h	W	DMA write request register
000Ah	R / W	DMA channel 0-3 mask register bits 7-3 = Reserved bit 2 = 0 Clear bit 1 Set bit bits 1-0 = Channel Select 00 Channel 0 01 Channel 1 10 Channel 2 11 Channel 3

I/O Address	Read/Write Status	Description
00Bh	W	DMA channel 0-3 mode register bits 7-6 = 00 Demand mode 01 Single mode 10 Block mode 11 Cascade mode bit 5 = 0 Address increment select 1 Address decrement select bit 4 = 0 Disable auto initialization 1 Enable auto initialization bits 3-2 = Operation type 00 Verify operation 01 Write to memory 10 Read from memory 11 Reserved bits 1-0 = Channel select 00 Channel 0 01 Channel 1 10 Channel 2 11 Channel 3
000Ch	W	DMA clear byte pointer flip/flop
000Dh	R	DMA read temporary register
000Dh	W	DMA master clear
000Eh	W	DMA clear mask register
000Fh	W	DMA write mask register
0020h	W	Programmable Interrupt Controller - Initialization Command Word 1 (ICW1) provided bit 4 = 1 bits 7-5 = 000 Used only in 8080 or 8085 mode bit 4 = 1 ICW1 is used bit 3 = 0 Edge triggered mode 1 Level triggered mode bit 2 = 0 Successive interrupt vectors separated by 8 bytes 1 Successive interrupt vectors separated by 4 bytes bit 1 = 0 Cascade mode 1 Single mode bit 0 = 0 ICW4 not needed 1 ICW4 needed
0021h	W	Used for ICW2, ICW3, or ICW4 in sequential order after ICW1 is written to port 0020h <b>ICW2</b> bits 7-3 = Address A0-A3 of base vector address for interrupt controller bits 2-0 = Reserved (should be 000) <b>ICW3</b> (for slave controller 00A1h) bits 7-3 = Reserved (should be 0000) bits 2-0 = 1 Slave ID <b>ICW4</b> bits 7-5 = Reserved (should be 000) bit 4 = 0 No special fully nested mode 1 Special fully nested mode bits 3-2 = Mode 00 Non buffered mode 01 Non buffered mode 10 Buffered mode/slave 11 Buffered mode/master bit 1 = 0 Normal EOI 1 Auto EOI bit 0 = 0 8085 mode 1 8080 / 8088 mode

I/O Address	Read/Write Status	Description
0021h	R / W	PIC master interrupt mask register (OCW1) bit 7 = 0 Enable parallel printer interrupt bit 6 = 0 Enable diskette interrupt bit 5 = 0 Enable hard disk interrupt bit 4 = 0 Enable serial port 1 interrupt bit 3 = 0 Enable serial port 2 interrupt bit 2 = 0 Enable video interrupt bit 1 = 0 Enable keyboard/pointing device/RTC interrupt bit 0 = 0 Enable interrupt timer
0021h	W	PIC OWC2 (if bits 4-3 = 0) bit 7 = Reserved bits 6-5 = 000 Rotate in automatic EOI mode (clear) 001 Nonspecific EOI 010 No operation 011 Specific EOI 100 Rotate in automatic EOI mode (set) 101 Rotate on nonspecific EOI command 110 Set priority command 111 Rotate on specific EOI command bits 4-3 = Reserved (should be 00) bits 2-0 = Interrupt request to which the command applies
0020h	R	PIC interrupt request and in-service registers programmed by OCW3 <b>Interrupt request register</b> bits 7-0 = 0 No active request for the corresponding interrupt line 1 Active request for the corresponding interrupt line <b>Interrupt in-service register</b> bits 7-0 = 0 Corresponding interrupt line not currently being serviced 1 Corresponding interrupt line is currently being serviced
0021h	W	PIC OCW3 (if bit 4 = 0, bit 3 = 1) bit 7 = Reserved (should 0) bits 6-5 = 00 No operation 01 No operation 10 Reset special mask 11 Set special mask bit 4 = Reserved (should be 0) bit = Reserved (should be 1) bit 2 = 0 No poll command 1 Poll command bits 1-0 = 00 No operation 01 Operation 10 Read interrupt request register on next read at port 0020 h 11 Read interrupt in-service register on next read at port 0020h
0022h	R / W	Chipset Register Address
0023h	R / W	Chipset Register Data
0040h	R / W	Programmable Interrupt Timer - read/write counter 0, keyboard controller channel 0
0041h	R / W	Programmer Interrupt Timer - channel 1
0042h	R / W	Programmable Interrupt Timer - miscellaneous register channel 2

I/O Address	Read/Write Status	Description
0043h	W	Programmable Interrupt Timer mode port - control word register for counters 0 and 2 bits 7-0 = Counter select 00 Counter 0 select 01 Counter 1 select 10 Counter 2 select bits 5-4 = 00 Counter latch command 01 R / W counter, bits 0-7 only 10 R / W counter, bits 8-15 only 11 R / W counter, bits 0-7 first, then bits 8-15 bits 3-1 = Select mode 000 Mode 0 001 Mode 1 programmable one shot x10 Mode 2 rate generator x11 Mode 3 square wave generator 100 Mode 4 software-triggered strobe 101 Mode 5 hardware-triggered strobe bit 0 = 0 Binary counter is 16 bits 1 Binary counter decimal (BCD) counter
0048h	R / W	Programmable Interrupt Timer
0060h	R	Keyboard Controller data port or keyboard input buffer
0060h	W	Keyboard or Keyboard Controller data output buffer
0064h	R	Keyboard Controller read status bit 7 = 0 No parity error 1 Parity error on keyboard transmission bit 6 = 0 No timeout 1 Received timeout bit 5 = 0 No timeout 1 Keyboard transmission timeout bit 4 = 0 Keyboard inhibited 1 Keyboard not inhibited bit 3 = 0 Data 1 Command bit 2 = System flag status bit 1 = 0 Input buffer empty 1 Input buffer full bit 0 = 0 Output buffer empty 1 Output buffer full
0064h	W	Keyboard Controller input buffer
0070h	R	CMOS RAM index register port and NMI mask bit 7 = 1 NMI disabled bits 6-0 = 0 CMOS RAM index
0071h	R / W	CMOS RAM data register port
0080h	R / W	Temporary storage for additional page register
0080h	R	Manufacturing diagnostic port (this port can access POST checkpoints)
0081h	R / W	DMA channel 2 address byte 2
0082h	R / W	DMA channel 2 address byte 2
0083h	R / W	DMA channel 1 address byte 2
0084h	R / W	Extra DMA page register
0085h	R / W	Extra DMA page register
0086h	R / W	Extra DMA page register
0087h	R / W	DMA channel 0 address byte 2
0088h	R / W	Extra DMA page register
0089h	R / W	DMA channel 6 address byte 2
008Ah	R / W	DMA channel 7 address byte 2
008Bh	R / W	DMA channel 5 address byte 2
008Ch	R / W	Extra DMA page register
008Dh	R / W	Extra DMA page register
008Eh	R / W	Extra DMA page register

I/O Address	Read/Write Status	Description
008Fh	R / W	DMA refresh page register
00A0h - 00A1h are reserved for the slave programmable interrupt controller. The bit definitions are identical to those of addresses 0020h - 0021h except where indicated.		
00A0h	R / W	Programmable interrupt controller 2
00A1h	R / W	Programmable interrupt controller 2 mask bit 7 = 0 Reserved bit 6 = 0 Enable hard disk interrupt bit 5 = 0 Enable coprocessor execution interrupt bit 4 = 0 Enable mouse interrupt bits 3-2 = 0 Reserved bit 1 = 0 Enable redirect cascade bit 0 = 0 Enable real time clock interrupt
00C0h	R / W	DMA channel 4 memory address bytes 1 and 0 (low)
00C2h	R / W	DMA channel 4 transfer count bytes 1 and 0 (low)
00C4h	R / W	DMA channel 5 memory address bytes 1 and 0 (low)
00C6h	R / W	DMA channel 5 transfer count bytes 1 and 0 (low)
00C8h	R / W	DMA channel 6 memory address bytes 1 and 0 (low)
00CAh	R / W	DMA channel 6 transfer count bytes 1 and 0 (low)
00CCh	R / W	DMA channel 7 memory address bytes 1 and 0 (low)
00CEh	R / W	DMA channel 7 transfer count bytes 1 and 0 (low)
00D0h	R	Status register for DMA channels 4-7 bit 7 = 1 Channel 7 request bit 6 = 1 Channel 6 request bit 5 = 1 Channel 5 request bit 4 = 1 Channel 4 request bit 3 = 1 Terminal count on channel 7 bit 2 = 1 Terminal count on channel 6 bit 1 = 1 Terminal count on channel 5 bit 0 = 1 Terminal count on channel 4
00D0h	W	Command register for DMA channels 4-7 bit 7 = 0 DACK sense active low 1 DACK sense active high bit 6 = 0 DREQ sense active low 1 DREQ sense active high bit 5 = 0 Late write selection 1 Extended write selection bit 4 = 0 Fixed Priority 1 Rotating Priority bit 3 = 0 Normal Timing 1 Rotating Timing bit 2 = 0 Enable controller 1 Disable controller bit 1 = 0 Disable memory-to-memory transfer 1 Enable memory-to-memory transfer bit 0 = Reserved
00D2h	W	Write request register for DMA channels 4-7
00D4h	W	Write single mask register bit for DMA channels 4-7 bits 7-3 = 0 Reserved bit 2 = 0 Clear mask bit 1 Set mask bit bits 1-0 = Channel select 00 Channel 4 01 Channel 5 10 Channel 6 11 Channel 7

I/O Address	Read/Write Status	Description
00D6h	W	Mode register for DMA channels 4-7 bits 7-6 = 00 Demand mode 01 Single mode 10 Block mode 11 Cascade mode bit 5 = 0 Address increment select 1 Address decrement select bit 4 = 0 Disable auto initialization 1 Enable auto initialization bits 3-2 = Operation type 00 Verify operation 01 Write to memory 10 Read from memory 11 Reserved bits 1-0 = Channel select 00 Channel 4 01 Channel 5 10 Channel 6 11 Channel 7
00D8h	W	Clear byte pointer flip/flop for DMA channels 4-7
00DAh	R	Read Temporary Register for DMA channels 4-7
00DAh	W	Master Clear for DMA channels 4-7
00DCh	W	Clear mask register for DMA channels 4-7
00DEh	W	Write mask register for DMA channels 4-7
00F0h	W	Math coprocessor clear busy latch
00F1h	W	Math coprocessor reset
00F2h - 00FFh	R / W	Math coprocessor
0140h - 014Fh	R / W	SCSI Controller if installed
I/O addresses 0170h - 0177h are reserved for use with a secondary hard drive. See addresses 01F0h - 01F7h for bit definitions.		
0170h	R / W	Data register for hard drive 1
0171h	R	Error register for hard drive 1
0171h	W	Pre-composition register for hard drive 1
0172h	R / W	Sector count - hard drive 1
0173h	R / W	Sector number for hard disk 1
0174h	R / W	Number of cylinders (low byte) for hard drive 1
0175h	R / W	Number of cylinders (high byte) for hard drive 1
0176h	R / W	Drive/head register for hard drive 1
0177h	R	Status register for hard drive 1
0177h	W	Command register for hard drive 1
01F0h	R / W	Data register base port for hard drive 0

I/O Address	Read/Write Status	Description
01F1h	R	Error register for hard drive 0 <b>Diagnostic mode</b> bits 7-3 = Reserved bits 2-0 = Errors 0001 No errors 0010 Controller error 0011 Sector buffer error 0100 ECC device error 0101 Control processor error <b>Operation mode</b> bit 7 = Block 0 Bad block 1 Block not bad bit 6 = Error 0 No error 1 Uncorrectable ECC error bit 5 = Reserved bit 4 = ID 0 ID located 1 ID not located bit 3 = Reserved bit 2 = Command 0 Completed 1 Not completed bit 1 = Track 000 0 Not found 1 Found bit 0 = DRAM 0 Not found 1 Found (CP-3022 always 0)
01F1h	W	Write pre-composition register for hard drive 0
01F2h	R / W	Sector count for hard disk 0
01F3h	R / W	Sector number for hard drive 0
01F4h	R / W	Number of cylinders (low byte) for hard drive 0
01F5h	R / W	Number of cylinders (high byte) for hard drive 0
01F6h	R / W	Drive/Head register for hard drive 0 bit 7 = 1 bit 6 = 0 bit 5 = 1 bit 4 = Drive select 0 First hard drive 1 Second hard drive bits 3-0 = Head select bits
01F7h	R	Status register for hard drive 0 bit 7 = 1 Controller is executing a command bit 6 = 1 Drive is ready bit 5 = 1 Write fault bit 4 = 1 Seek operation complete bit 3 = 1 Sector buffer requires servicing bit 2 = 1 Disk data read completed successfully bit 1 = Index (is set to 1 at each disk revolution) bit 0 = 1 Previous command ended with error
01F7h	W	Command register for hard drive 0
0200h - 020Fh	R / W	Game controller ports
0201h	R / W	I/O data - game port
0220h - 022Fh	R / W	Sound port AD1816 reserved
I/O addresses 0278h - 027Ah are reserved for use with parallel port 2. See the bit definitions for addresses 0378h - 037Ah.		
0278h	R / W	Data port for parallel port 2

I/O Address	Read/Write Status	Description
0279h	R	Status port for parallel port 2
0279h	W	PnP Address register (only for PnP devices)
027Ah	R / W	Control port for parallel port 2
02B0h - 02BFh	R / W	Digital I/O for Latch, WDOG, Control
I/O addresses 02E8h - 02EFh are reserved for use with serial port 4. See the bit definitions for I/O addresses 03F8h - 03FFh.		
02E8h	W	Transmitter holding register for serial port 4
02E8h	R	Receive buffer register for serial port 4
02E8h	R / W	Baud rate divisor (low byte) when DLAB = 1
02E9h	R / W	Baud rate divisor ( high byte) when DLAB = 1
02E9h	R / W	Interrupt enable register when DLAB = 0
02EAh	R	Interrupt identification register for serial port 4
02EBh	R / W	Line control register for serial port 4
02ECh	R / W	Modem control register for serial port 4
02EDh	R	Line status register for serial port 4
02EEh	R	Modem status register for serial port 4
02EFh	R / W	Scratch register for serial port 4 (used for diagnostics)
I/O addresses 02F8h - 02FFh are reserved for use with serial port 2. See the bit definitions for I/O addresses 03F8h - 03FFh.		
02F8h	W	Transmitter holding register for serial port 2
02F8h	R	Receive buffer register for serial port 2
02F8h	R / W	Baud rate divisor (low byte) when DLAB = 1
02F9h	R / W	Baud rate divisor ( high byte) when DLAB = 1
02F9h	R / W	Interrupt enable register when DLAB = 0
02FAh	R	Interrupt identification register for serial port 2
02FBh	R / W	Line control register for serial port 2
02FCh	R / W	Modem control register for serial port 2
02FDh	R	Line status register for serial port 2
02FEh	R	Modem status register for serial port 2
02FFh	R / W	Scratch register for serial port 2 (used for diagnostics)
0300h - 031Fh	R / W	ISA- LAN controller, if installed (otherwise is free for the user)
I/O addresses 0372h - 0377h are reserved for use with a secondary diskette controller. See the bit definitions for 03F2h - 03F7h.		
0372h	W	Digital output register for secondary diskette drive controller
0374h	R	Status register for secondary diskette drive controller
0375h	R / W	Data register for secondary diskette drive controller
0376h	R / W	Control register for secondary diskette drive controller
0377h	R	Digital input register for secondary diskette drive controller
0377h	W	Select register for secondary diskette data transfer rate
0378h	R / W	Data port for parallel port 1 bit 7 = 0 Busy bit 6 = 0 Acknowledge bit 5 = 1 Out of paper bit 4 = 1 Printer is selected bit 3 = 0 Error bit 2 = 0 IRQ has occurred bit 1-0 = Reserved
0379h	R / W	Status port for parallel port 1 bit 7 = 0 Busy bit 6 = 0 Acknowledge bit 5 = 1 Out of paper bit 4 = 1 Printer is selected bit 3 = 0 Error bit 2 = 0 IRQ has occurred bit 1-0 = Reserved

I/O Address	Read/Write Status	Description
037Ah	R / W	Control port for parallel port 1 bits 7-5 = Reserved bit 4 = 1 Enable IRQ bit 3 = 1 Select printer bit 2 = 0 Initialize printer bit 1 = 1 Automatic line feed bit 0 = 1 Strobe
03B0h - 03B8h	R / W	Various video registers
I/O addresses 03BCh - 03BEh are reserved for use with parallel port 3. See the bit definitions for addresses 0378h - 037Ah.		
03BCh	R / W	Data port - parallel port 3
03BDh	R / W	Status port - parallel port 3
03BEh	R / W	Control port - parallel port 3
03C0h - 03CFh	R / W	Video subsystem (EGA/VGA)
03C2h - 03D9h	R / W	Various CGA and CRTC registers
03E0h	R / W	PCCARD Address select
03E1h	R / W	PCCARD Data transfer with 365SL controller
I/O addresses 03E8h - 03EFh are reserved for use with serial port 3. See the bit definitions for I/O addresses 03F8h - 03FFh.		
03E8h	W	Transmitter holding register for serial port 3
03E8h	R	Receive buffer register for serial port 3
03E8h	R / W	Baud rate divisor (low byte) when DLAB = 1
03E9h	R / W	Baud rate divisor ( high byte) when DLAB = 1
03E9h	R / W	Interrupt enable register when DLAB = 0
03EAh	R	Interrupt identification register for serial port 3
03EBh	R / W	Line control register for serial port 3
03ECh	R / W	Modem control register for serial port 3
03EDh	R	Line status register for serial port 3
03EEh	R	Modem status register for serial port 3
03EFh	R / W	Scratch register for serial port 3 (used for diagnostics)
03F2h	W	Digital output register for primary diskette drive controller bits 7-6 = 0 Reserved bit 5 = 1 Enable drive 1 motor bit 4 = 1 Enable drive 0 motor bit 3 = 1 Enable diskette DMA bit 2 = 0 Reset controller bit 1 = 0 Reserved bit 0 = 0 Select drive 0 1 Select drive 1
03F4h	R	Status register for primary diskette drive controller bit 7 = 1 Data register is ready bit 6 = 0 Transfer from system to controller 1 Transfer from controller to system bit 5 = 1 Non-DMA mode bit 4 = 1 Diskette drive controller is busy bits 3-2 = Reserved bit 1 = 1 Drive 1 is busy bit 0 = 1 Drive 0 is busy
03F5h	R / W	Data register for primary diskette drive controller
03F6h	R	Control port for primary diskette drive controller bits 7-4 = Reserved bit 3 = 0 Reduce write current 1 Head select enable bit 2 = 0 Disable diskette drive reset 1 Enable diskette drive reset bit 1 = 0 Disable diskette drive initialization 1 Enable diskette drive initialization bit 0 = Reserved

I/O Address	Read/Write Status	Description
03F7h	R	Digital input register for primary diskette drive controller bit 7 = 1 Diskette drive line change bit 6 = 1 Write gate bit 5 = Head select 3 / reduced write current bit 4 = Head select 2 bit 3 = Head select 1 bit 2 = Head select 0 bit 1 = Drive 1 select bit 0 = Drive 0 select
03F7h	W	Select register for primary diskette data transfer rate bits 7-2 = Reserved bits 1-0 = 00 500 Kbs mode 01 300 Kbs mode 10 250 Kbs mode 11 Reserved
I/O addresses 03F8h - 03FFh are reserved for use with serial port 1. The bit definitions for these addresses also apply to serial ports 2, 3, and 4.		
03F8h	W	Transmitter holding register for serial port 1 - Contains the character to be sent. Bit 0, the least significant bit, is the first bit sent. bits 7-0 = Data bits 0-7 when the Divisor Latch Access Bit (DLAB) is 0
03F8h	R	Receive buffer register for serial port 1 - Contains the character to be received. Bit 0, the least significant bit, is the first bit received. bits 7-0 = Data bits 0-7 when the Divisor Latch Access Bit (DLAB) is 0
03F8h	R / W	Baud rate divisor (low byte) - This byte, along with the high byte (03F9h), store the data transmission rate divisor. bits 7-0 = Data bits 0-7 when the Divisor Latch Access Bit (DLAB) is 1
03F9h	R / W	Baud rate divisor (high byte) - This byte, along with the low byte (03F8h), store the data transmission rate divisor. bits 7-0 = Bits 8-15 when DLAB = 1
03F9h	R / W	Interrupt enable register bits 7-4 = Reserved bit 3 = 1 Modem status interrupt enable bit 2 = 1 Receiver line status interrupt enable bit 1 = 1 Transmitter holding register empty interrupt enable bit 0 = 1 Received data available interrupt enable when DLAB = 0
03FAh	R	Interrupt identification register - serial port 1 bits 7-3 = Reserved bits 2-1 = Identify interrupt with highest priority 00 Modem status interrupt (4th priority) 01 Transmitter holding register empty (3rd priority) 10 Received data available (2nd priority) 11 Receiver line status interrupt (1st priority) bit 0 = 0 Interrupt pending (register contents can be used as a pointer to interrupt service routine) 1 No interrupt pending

I/O Address	Read/Write Status	Description
03FBh	R / W	Line control register - serial port 1 bit 7 = Divisor Latch Access (DLAB) 0 Access receiver buffer, transmitter holding register, and interrupt enable register 1 Access divisor latch bit 6 = 1 Set break enable. Forces serial output to spacing state and remains there bit 5 = Stick parity bit 4 = Even parity select bit 3 = Parity enable bit 2 = Number of stop bits bit 1 = Word length 00 5-bit word length 01 6-bit word length 10 7-bit word length 11 8-bit word length
03FCh	R / W	Modem control register - serial port 1 bits 7-5 = Reserved bit 4 = 1 Loopback mode for diagnostic testing of serial port. bit 3 = 1 User-defined output 2 bit 2 = 1 User-defined output 1 bit 1 = Force Request To Send active bit 0 = Force Data Terminal Ready active
03FDh	R	Line status register - serial port 1 bit 7 = Reserved bit 6 = 1 Transmitting shift and holding registers empty bit 5 = 1 Transmitter shift register empty bit 4 = 1 Break interrupt bit 3 = 1 Framing error bit 2 = 1 Overrun error bit 0 = 1 Data ready
03FEh	R	Modem status register - serial port 1 bit 7 = 1 Data Carrier Detect bit 6 = 1 Ring Indicator bit 5 = 1 Data Set Ready bit 4 = 1 Clear To Send bit 3 = 1 Delta Data Carrier bit 2 = 1 Trailing Edge Ring Indicator bit 1 = 1 Delta Data Set Ready bit 0 = 1 Delta Clear To Send
03FFh	R / W	Scratch register - serial port 1 (used for diagnostics)
0A79h	W	PnP Data write register (only for PnP devices)

## 5. VGA/LCD

### 5.1. VGA / LCD ATI M1

The RAGE™ MOBILITY™ M1, ATI's third generation of graphics and multimedia accelerators, offers an extensive feature set, up to 8MB of integrated memory, and low power consumption while delivering outstanding performance.

#### Features:

- **Process technology, Core Voltage:** 0.25um, 2.5V
  - **Graphics Clock:** 83 MHz
- **Memory Type:** NEC 1MBx16 SDRAM (M & M1); Micron 1MBx16 SDRAM (M1)
  - **I/O Type, VDDC:** SSTL, 3.3V
  - **Memory Clock, Max Memory Path:** 125 MHz clock, 64 bit width
  - **Maximum Memory Configuration:** 8 MB (Mob. M1 = 8MB int.)
- **Outputs**
  - **CRT1 (Primary):** Triple 8-bit palette DAC, 230MHz
  - **CRT1 (Secondary):** Triple 8-bit palette DAC
  - **Integrated LVDS:** Dual Channel LVDS up to 112 MHz per channel
    - Supports 18 bit and 24 bit modes for both single and dual channel LVDS.
    - TFT & DSTN Panel support
  - **Integrated TV encoder:** Shares the Secondary DAC
  - **DVO (TTL):** Supports 18/24 bit SDR mode
  - **Supported Display Combinations:** LVDS + CRT/TV
- **Resolution Support**
  - **Max 2D/3D resolution:** 8MB: 1600x1200/1280x1024;
  - **Max color depth:** 16.7M Colors
  - **LVDS, TV-out:** 1280x1024, 1024x768
- **Driver Support**
  - Win 98/ME/2000/XP/NT, Linux (Please see your technical contact for alternate OS support)
- **Video Support**
  - Video on graphics overlay, color space conversion (YUV to RGB)
  - MPEG-2 hardware decode acceleration
- **Brief Overview of 2D/3D Support**
  - Hardware acceleration of BitBlit, Line Draw, Polygon/Rectangle fill, Bit Masking
  - Complete 3D primitive support, edge anti-aliasing, gouraud, specular shading, texture mapping

#### CRT Controller (CRTC)

The CRTC subsystem has additional enhancements such as support for overscan, video memory sizes up to 8MB, and screen resolutions up to 1920x1080, non-interlaced.

#### Display Controller #1 (Primary)

The primary display controller subsystem consists of four subunits as follows:

- Display FIFO #1 to manage the memory interface for displayed pixel data.
- Enhanced attribute controller for VGA.
- The primary display controller.
- 24-bit primary palette.

This display controller subsystem supports VGA graphic modes up to 1600x1200 (85Hz), VGA text modes up to 132-column on a PS/2 monitor, and accelerator display modes up to 1600x1200 (85Hz) and 1920x1080 (72Hz).

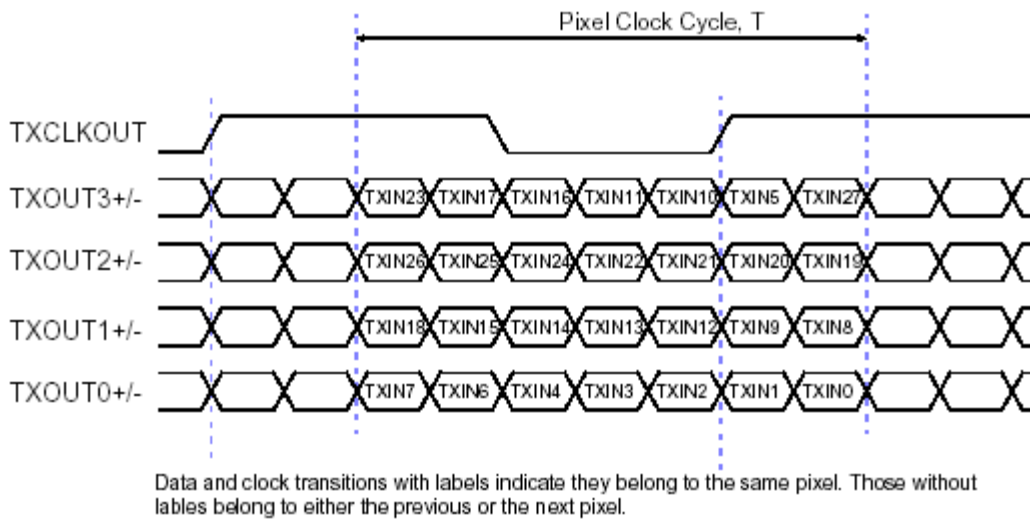
## 5.2. Comparison Chart VGA Controller

	Rage Mobility M1	Asilant 69000
Memory Speed	125Mhz	83Mhz
Memory Size	8MB	2MB
DAC Speed	230Mhz	135Mhz
3D Support	Yes	No
Integrated LVDS Support	Yes	No
Dual Display	Yes	No
Independent CRT/DVO	Yes	No
Independent CRT/TV	Yes	No
Availability Guarantee	5 years till 2008	Last-time buy

## 5.3. TFT Panel Mapping

LCD DATA Pins	TFT (XGA) 9-bit	TFT (XGA) 12-bit	TFT (XGA) Config1 18-bit	TFT (XGA) Config2 18-bit	TFT (SGA/XGA) 24-bit
LCDDO0	UR0	UR0		R0	R0
LCDDO1	UR1	UR1		R1	R1
LCDDO2	UR2	UR2	R0	R2	R2
LCDDO3	LR0	UR3	R1	R3	R3
LCDDO4	LR1	LR0	R2	R4	R4
LCDDO5	LR2	LR1	R3	R5	R5
LCDDO6	UG0	LR2	R4		R6
LCDDO7	UG1	LR3	R5		R7
LCDDO8	UG2	UG0		G0	G0
LCDDO9	LG0	UG1		G1	G1
LCDDO10	LG1	UG2	G0	G2	G2
LCDDO11	LG2	UG3	G1	G3	G3
LCDDO12	UB0	LG0	G2	G4	G4
LCDDO13	UB1	LG1	G3	G5	G5
LCDDO14	UB2	LG2	G4		G6
LCDDO15	LB0	LG3	G5		G7
LCDDO16	LB1	UB0		B0	B0
LCDDO17	LB2	UB1		B1	B1
LCDDO18		UB2	B0	B2	B2
LCDDO19		UB3	B1	B3	B3
LCDDO20	LTGIO3	LB0	B2	B4	B4
LCDDO21	LTGIO4	LB1	B3	B5	B5
LCDDO22	LTGIO5	LB2	B4		B6
LCDDO23	LTGIO6	LB3	B5		B7

## 5.4. LVDS Data/Clock Mapping



## 5.5. LVDS Pin Multiplexing

Pin Name	LVDS signal	Channel
LCDDO0	Txout0-	first
LCDDO1	Txout0+	first
LCDDO2	Txout1-	first
LCDDO3	Txout1+	first
LCDDO4	Txout2-	first
LCDDO5	Txout2+	first
LCDDO6	Txclk-	first
LCDDO7	Txclk+	first
LCDDO8	Txout3-	first
LCDDO9	Txout3+	first
LCDDO10	Txout0-	second
LCDDO11	Txout0+	second
LCDDO12	Txout1-	second
LCDDO13	Txout1+	second
LCDDO14	Txout2-	second
LCDDO15	Txout2+	second
LCDDO16	Txclk-	second
LCDDO17	Txclk+	second
LCDDO18	Txout3-	second
LCDDO19	Txout3+	second

## 5.6. LVDS TFT Interface 18bit Single Pixel per Clock

TX Signal	Pin (Data)	TX Signal	Pin (Data)
TxIN0	R0	TxIN11	G5
TxIN1	R1	TxIN12	B0
TxIN2	R2	TxIN13	B1
TxIN3	R3	TxIN14	B2
TxIN4	R4	TxIN15	B3
TxIN5	R5	TxIN16	B4
TxIN6	G0	TxIN17	B5
TxIN7	G1	TxIN18	HSYNC
TxIN8	G2	TxIN19	VSYNC
TxIN9	G3	TxIN20	ENABLE
TxIN10	G4	TxCLK IN	CLOCK

## 5.7. Display Modes without DVD/Video Overlay & 3D

Display Resolution	Refresh (Hz)	Colour Depth			
		8 bpp	16 bpp	24 bpp	32 bpp
640x480	60	Yes	Yes	Yes	Yes
	75	Yes	Yes	Yes	Yes
	85	Yes	Yes	Yes	Yes
	100	Yes	Yes	Yes	Yes
800x600	60	Yes	Yes	Yes	Yes
	75	Yes	Yes	Yes	Yes
	85	Yes	Yes	Yes	Yes
	100	Yes	Yes	Yes	Yes
1024x768	60	Yes	Yes	Yes	Yes
	75	Yes	Yes	Yes	Yes
	85	Yes	Yes	Yes	Yes
	100	Yes	Yes	Yes	Yes
1280x1024	60	Yes	Yes	Yes	Yes
	75	Yes	Yes	Yes	Yes
	85	Yes	Yes	Yes	Yes
	100	Yes	Yes	Yes	Yes
1600x1200	60	Yes	Yes	Yes	Yes
	75	Yes	Yes	Yes	Yes
	85	Yes	Yes	Yes	Yes
	100	Yes	Yes	Yes	-

## 5.8. DVD Modes

Table 7-22 Mobility M/P 8MB: Single Display Mode Support (CRT/TFT, SW DVD, iDCT and Subpicture)

Display Resolution	Refresh (Hz)	Colour Depth Supported - NTSC				Colour Depth Supported - PAL			
		8 bpp	16 bpp	24 bpp	32 bpp	8 bpp	16 bpp	24 bpp	32 bpp
640x480	60	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	75	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	85	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	100	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
800x600	60	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	75	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	85	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	100	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1024x768	60	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	75	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	85	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	100	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1280x1024	60	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	75	Yes	Yes	Yes	-	Yes	Yes	Yes	-
	85	Yes	Yes	-	-	Yes	Yes	-	-
	100	-	-	-	-	-	-	-	-

## 5.9. 3D Modes

Table 7-26 Mobility M/P 8MB: Single Display Full Screen 3D Mode Support (TFT/CRT)

Display Resolution	Colour Depth:			
	8 bpp	16 bpp	24 bpp	32 bpp
640x480	Yes	Yes	Yes	Yes
800x600	Yes	Yes	Yes	Yes
1024x768	Yes	Yes	Yes	Yes
1280x1024	Yes	Yes	-	-
1600x1200	Yes	-	-	-

## 5.10. VGA/LCD BIOS Support

Each LCD display needs a specifically adapted VGA-BIOS. This product is equipped with the CRT standard VGA-BIOS.

To connect an LCD display to this product, you need to perform the following:

Check the LCD\_OVERVIEW.PDF to see if the LCD BIOS is available.  
Get the latest VGA-BIOS from our website <http://www.digitallogic.com>

### **IF THE LCD BIOS IS AVAILABLE:**

1. A description of the connection between the LCD and this product is described in the FLATPANEL-SUPPORT documentation.
2. DOWNLOAD the corresponding LCD-BIOS with the special utility.  
Go to the following section, 5.11 "Download the VGA-BIOS", and follow those steps.
3. Restart the system and check the VGA-BIOS header message. The LCD name must be visible though only for a short time. The VGA-BIOS message appears as the first info page on the screen.
4. Stop the system, connect the LCD to the system and restart.
5. If, on the LCD, no image appears – as soon as the monitor begins to show the first text, stop the system immediately, ***otherwise the LCD will be damaged.***
6. Check the LCD connection again.



### **FOR A NEW LCD TYPE, NOT CURRENTLY AVAILABLE:**

If the LCD BIOS for your LCD is not available, DIGITAL-LOGIC will adapt the LCD and provide you with a working cable. For this we need the following:

1. An order to adapt the LCD (ask your sales contact for the costs).
2. Send us the LCD panel, a datasheet, a connector to the LCD and the inverter for the backlight.

### **LCD types:**

#### **Possible:**

LVDS TFT 18bit / 24bit	640x480 to 1600x1280
LVDS TFT 2x18bit / 2x24bit (double pixel per Clock)	640x480 to 1600x1280
LVDS DSTN Pack 12x2 / Pack 8x2	640x480 to 1280x1024
TFT 9bit / 12bit / 18bit / 24bit	640x480 to 1600x1280
STN Single Panel Pack 12 / Pack 16	640x480 to 1280x1024
STN Split Panel Pack 6 / Pack 8 / Pack 12	640x480 to 1280x1024

LCD and TV-Out together

#### **Not Possible:**

320x240 QVGA 1/4VGA  
LCD with less than 12bit Data  
Monochrome LCD (black & white)  
Analog LCD  
DVI and LCD together



### ***ATTENTION!***

DIGITAL-LOGIC AG is never responsible for a damaged LCD display. Even when there are mistakes in the BIOS or in any documentation for the LCD.

## 5.11. Download the VGA-BIOS

Before downloading an ATI VGA-BIOS, please check the following:

Make a bootable diskette that includes the following files:

- FLASHROM.EXE
- "VGA"bios.bin



### **NOTE...**

Do not use boot disks created in a Windows operating system. If you do not have an MSDOS 6.22 disk available, you can download a boot disk from [www.bootdisk.com](http://www.bootdisk.com).

### **Start the DOWNLOADING process:**

1. Start the system with the bootable diskette. If you do not have a bootable diskette or floppy drive, you can start in DOS-mode by pressing the **F5** key to disable autoexec.bat and config.sys.
2. Run: flashrom -p 0 filename.bin
3. Switch off the system after the download is finished



### **IMPORTANT:**

*If you use the MSMP\_SEG-DVICON with a DVI monitor, you must flash the M1\_DVI.bin bios.*

*If you use the MSMP\_SEG-DVICON with the TV-Output, you mustflash the M1\_TV.bin bios.*

*If you want to use the LAN BOOT function, you must flash the ATIM132K.bin bios (no VESA support).*

VGA-BIOS	Size	LAN BOOT (32k)	
		Possible	Not possible
M1_DVI.bin	64k		X
M1_TV.bin	64k		X
ATIM132K.bin	32k	X	

(Total ROM size = 64k)

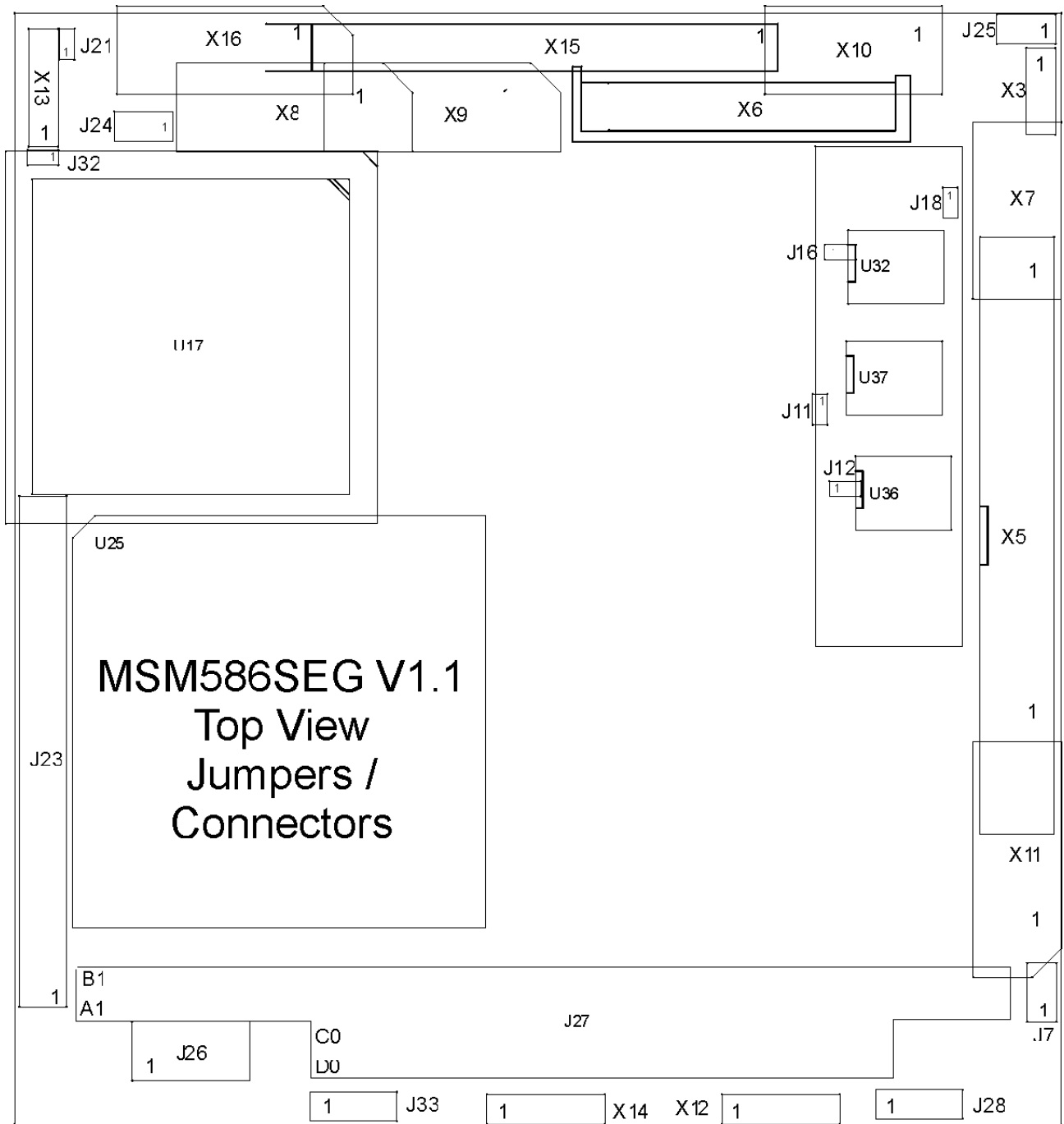
## 6. DESCRIPTION OF THE CONNECTORS

### Flat cable

- 44pin IDE is: IDT Terminal for Dual Row (2.00mm grid) and 1.00mm flat cable
- All others are: IDT Terminal for Dual Row 0.1" (2.54mm grid) and 1.27mm flat cable

Connector	Structure	Pin	Remarks
J23	HDD primary	2x22	2mm
J25	External HDD LED	2	2.54mm
J26	Power supply / IrDA	8	2.54mm
J27	PC104 bus	104	2.54mm
U20	SODIMM socket	144	
U21	CompactFlash Type1	50	
U41	DOC2000 IC socket	2x16	2.54mm
X2	JTAG connector	2x6	2mm
X3	LAN LED connector	3	2.54mm
X5	LPT	2x13	2.54mm
X6	FDD Micro	26	FCC micro
X7	COM A (ELAN520)	2x5	2.54mm
X8	COM D (SUPER I/O)	2x5	2.54mm
X9	COM C (SUPER I/O)	2x5	2.54mm
X10	COM B (ELAN520)	2x5	2.54mm
X11	Utility; PS/2 Mouse/Keyboard; Reset; Speaker	2x5	2.54mm
X12	USB 1.1 Channel 2	4	2.54
X13	LAN	4	2.54mm
X14	USB 1.1 Channel 1	4	2.54
X15	LCD / TV-Out	2x20	2mm
X16	VGA / CRT	2x5	2.54

Connector Plan MSM586SEG/SEL V1.1/V1.2



**J23 IDE Interface**

Pin	Signal	Pin	Signal
1	Reset (active low)	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	(keypin) <b>NC</b>
21	<b>NC</b>	22	GND
23	IOW (active low)	24	GND
25	IOR (active low)	26	GND
27	IOCHRDY (active low)	28	(ALE / Master-Slave) <b>NC</b>
29	<b>NC</b>	30	GND
31	IRQ	32	IOCS16 (active low)
33	ADR1	34	<b>NC</b>
35	ADR0	36	ADR2
37	CS0 (active low)	38	CS1 (active low)
39	LED (active low)	40	GND
41	VCC Logic	42	VCC Motor
43	GND	44	<b>NC</b>

**J25 External HDD LED (new since V2.2)**

Pin	Signal	Pin	Signal
1	VCC	2	HDD

**J26 Power Supply / IrDA**

Pin	Signal	Pin	Signal
1	GND	2	VCC (+5V)
3	NC	4	+12Volt (for LCD backlight)
5	Fast IrDA_TX (TTL)	6	Fast IrDA_RX (TTL)
7	GND	8	VCC (+5V)

**Remarks:**

Fast IrDA is directly connected to the SUPER I/O (TX=Pin 82; RX= Pin 81).  
Drivers must be written by the customer.

**J27 PC/104 BUS Interface**

Pin	A:	B:	C:	D:
0			Ground	Ground
1	(IOCHCK) NC	Ground	SBHE	MEMCS16
2	SD7	RESET	LA23	IOCS16
3	SD6	(+5V) NC	LA22	IRQ10
4	SD5	IRQ9	LA21	IRQ11
5	SD4	NC	LA20	IRQ12
6	SD3	DRQ2	LA19	IRQ15
7	SD2	(-12V) NC	LA18	IRQ14
8	SD1	(OWS) NC	LA17	DACK0
9	SD0	+12V	MEMR	DRQ0
10	IOCHRDY	(Ground) NC	MEMW	DACK5
11	AEN	SMEMW	SD8	DRQ5
12	SA19	SMEMR	SD9	DACK6
13	SA18	SIOW	SD10	DRQ6
14	SA17	SIOR	SD11	DACK7
15	SA16	DACK3	SD12	DRQ7
16	SA15	DRQ3	SD13	+5 Volt
17	SA14	DACK1	SD14	(MASTER) NC
18	SA13	DRQ1	SD15	Ground
19	SA12	(REF) **	Ground	Ground
20	SA11	(SYSCLK) *		
21	SA10	IRQ7		
22	SA9	IRQ6		
23	SA8	IRQ5		
24	SA7	IRQ4		
25	SA6	IRQ3		
26	SA5	DACK2		
27	SA4	TC		
28	SA3	ALE		
29	SA2	+5 Volt		
30	SA1	OSC 14MHz		
31	SA0	Ground		
32	Ground	Ground		

\* SYSCLK is 8.25MHz, available since V2.2

\*\* REFGRESH is pulled up to VCC with 1 k $\Omega$

**Signals used onboard (not for external use):**

IRQ3, IRQ4	COM1/2
IRQ7	LPT1
IRQ6	FD
<b>IRQ10</b>	<b>HD (BIOS setup depending)</b>
IRQ14	HD
IRQ12	PS/S Mouse
IRQ13	Co-processor
TC	FD
DACK2 and DRQ2	FD
DRQ9/10	COM3/4

**U20 SODIMM (Small Outline- Dual Inline Memory Module), 144pins**

Information taken from "The Hardware Book"

Pin	Normal	Description	Pin	Normal	Description
1	VSS	Ground	73	/OE	
2	VSS	Ground	74	NC	NC
3	DQ0	Data 0	75	VSS	Ground
4	DQ32	Data 32	76	VSS	Ground
5	DQ1	Data 1	77	NC	
6	DQ33	Data 33	78	NC	
7	DQ2	Data 2	79	NC	
8	DQ34	Data 34	80	NC	
9	DQ3	Data 3	81	VCC	+5 VDC
10	DQ35	Data 35	82	VCC	+5 VDC
11	VCC	+5 VDC	83	DQ16	Data 16
12	VCC	+5 VDC	84	DQ48	Data 48
13	DQ4	Data 4	85	DQ17	Data 17
14	DQ36	Data 36	86	DQ49	Data 49
15	DQ5	Data 5	87	DQ18	Data 18
16	DQ37	Data 37	88	DQ50	Data 50
17	DQ6	Data 6	89	DQ19	Data 19
18	DQ38	Data 38	90	DQ51	Data 51
19	DQ7	Data 7	91	VSS	Ground
20	DQ39	Data 39	92	VSS	Ground
21	VSS	Ground	93	DQ20	Data 20
22	VSS	Ground	94	DQ52	Data 52
23	/CAS0	Column Address Strobe 0	95	DQ21	Data 21
24	/CAS4	Column Address Strobe 4	96	DQ53	Data 53
25	/CAS1	Column Address Strobe 1	97	DQ22	Data 22
26	/CAS5	Column Address Strobe 5	98	DQ54	Data 54
27	VCC	+5 VDC	99	DQ23	Data 23
28	VCC	+5 VDC	100	DQ55	Data 55
29	A0	Address 0	101	VCC	+5 VDC
30	A3	Address 3	102	VCC	+5 VDC
31	A1	Address 1	103	A6	Address 6
32	A4	Address 4	104	A7	Address 7
33	A2	Address 2	105	A8	Address 8
34	A5	Address 5	106	A11	Address 11
35	VSS	Ground	107	VSS	Ground
36	VSS	Ground	108	VSS	Ground
37	DQ8	Data 8	109	A9	Address 9
38	DQ40	Data 40	110	A12	Address 12
39	DQ9	Data 9	111	A10	Address 10
40	DQ41	Data 41	112	A13	Address 13
41	DQ10	Data 10	113	VCC	+5 VDC
42	DQ42	Data 42	114	VCC	+5 VDC
43	DQ11	Data 11	115	/CAS2	Column Address Strobe 2
44	DQ43	Data 43	116	/CAS6	Column Address Strobe 6
45	VCC	+5 VDC	117	/CAS3	Column Address Strobe 3
46	VCC	+5 VDC	118	/CAS7	Column Address Strobe 7
47	DQ12	Data 12	119	VSS	Ground
48	DQ44	Data 44	120	/VSS	Ground
49	DQ13	Data 13	121	DQ24	Data 24
50	DQ45	Data 45	122	DQ56	Data 56
51	DQ14	Data 14	123	DQ25	Data 25
52	DQ46	Data 46	124	DQ57	Data 57
53	DQ15	Data 15	125	DQ26	Data 26
54	DQ47	Data 47	126	DQ58	Data 58
55	VSS	Ground	127	DQ27	Data 27
56	VSS	Ground	128	DQ59	Data 59
57	NC		129	VCC	+5 VDC
58	NC		130	VCC	+5 VDC
59	NC		131	DQ28	Data 28
60	NC		132	DQ60	Data 60
61	DU	Don't use	133	DQ29	Data 29
62	DU	Don't use	134	DQ61	Data 61
63	VCC	+5 VDC	135	DQ30	Data 30
64	VCC	+5 VDC	136	DQ62	Data 62
65	DU	Don't use	137	DQ31	Data 31
66	DU	Don't use	138	DQ63	Data 63
67	/WE	Read/Write	139	VSS	Ground
68	NC	Not connected	140	VSS	Ground
69	/RAS0	Row Address Strobe 0	141	SDA	
70	NC	Not connected	142	SCL	
71	/RAS1	Row Address Strobe 1	143	VCC	+5 VDC
72	NC	Not connected	144	VCC	+5 VDC

**U21 CompactFlash Holder, Type1**

Pin	Signal
1	GND
2	D3
3	D4
4	D5
5	D6
6	D7
7	CS0 (active low)
8	(A10) <b>GND</b>
9	GND
10	(A9) <b>GND</b>
11	(A8) <b>GND</b>
12	(A7) <b>GND</b>
13	VCC
14	(A6) <b>GND</b>
15	(A5) <b>GND</b>
16	(A4) <b>GND</b>
17	(A3) <b>GND</b>
18	ADR2
19	ADR1
20	ADR0
21	D0
22	D1
23	D2
24	IOCS16 (active low)
25	(CD2) <b>NC</b>
26	(CD1) <b>NC</b>
27	D11
28	D12
29	D13
30	D14
31	D15
32	CS1 (active low)
33	(VS1) <b>NC</b>
34	IOR (active low)
35	IOW (active low)
36	VCC
37	IRQ
38	VCC
39	CEL
40	(VS2) <b>NC</b>
41	Reset (active low)
42	IOCHRDY (active low)
43	(INPACK-) <b>NC</b>
44	VCC
45	LED (active low)
46	PDIAG
47	D8
48	D9
49	D10
50	GND

**Pin order (solder view)**

Pin 25	Pin 1
Pin 50	Pin 26

**U41 DOC 2000 IC-Socket**

Pin	Signal	Pin	Signal
1	NC	17	D3
2	A16	18	D4
3	A15	19	D5
4	A12	20	D6
5	A7	21	D7
6	A6	22	CE#
7	A5	23	A10
8	A4	24	OE#
9	A3	25	A11
10	A2	26	A9
11	A1	27	A8
12	A0	28	A13
13	D0	29	A14
14	D1	30	NC
15	D2	31	WE#
16	GND	32	VCC

**X2 JTAG Connector (debugging)**

Pin	Signal	Pin	Signal
1	GND	2	VCC
3	TCK	4	CMDACK
5	TMS	6	BREAK
7	TDI	8	STOP
9	TDO	10	TRACE
11	TRST	12	RESETIN

**X3 LAN LED**

Pin	Signal	Remarks
1	LILEDX / Link LED	330 Ohm resistor on board
2	VCC3	
3	ACTLEDX / Activity LED	330 Ohm resistor on board

**X5 Printer Port (Centronics)**

The printer connector provides an interface for 8bit Centronics printers.

Header onboard	D-SUB connector	Signal
Pin 1	Pin 1	Strobe
Pin 3	Pin 2	Data 0
Pin 5	Pin 3	Data 1
Pin 7	Pin 4	Data 2
Pin 9	Pin 5	Data 3
Pin 11	Pin 6	Data 4
Pin 13	Pin 7	Data 5
Pin 15	Pin 8	Data 6
Pin 17	Pin 9	Data 7
Pin 19	Pin 10	Acknowledge
Pin 21	Pin 11	Busy
Pin 23	Pin 12	Paper end
Pin 25	Pin 13	Select
Pin 2	Pin 14	Autofeed
Pin 4	Pin 15	Error
Pin 6	Pin 16	Init printer
Pin 8	Pin 17	Shift in (SI)
Pins 10, 12, 14, 16, 18	Pins 18 - 22	Left open
Pins 20, 22, 24	Pins 23 - 25	GND

**X6 Floppy Disk Interface- Connector (MOLEX 26pin FCC)**

FD26	Signal Name	Function	in/out
Pin 1	VCC	+5Volt	
Pin 2	IDX	Index Pulse	in
Pin 3	VCC	+5Volt	
Pin 4	DS2	Drive Select 2	out
Pin 5	VCC	+5Volt	
Pin 6	DCHG	Disk Change	in
Pin 10	M02	Motor On 2	out
Pin 12	DIRC	Direction Select	out
Pin 14	STEP	Step	out
Pin 16	WD	Write Data	out
Pin 17	GND	Signal grounds	
Pin 18	WE	Write Enable	out
Pin 19	GND	Signal grounds	
Pin 20	TRKO	Track 0	in
Pin 21	GND	Signal grounds	
Pin 22	WP	Write Protect	in
Pin 23	GND	Signal grounds	
Pin 24	RDD	Read Data	in
Pin 25	GND	Signal grounds	
Pin 26	HS	Head Select	out

**X7 Serial Port COMA (from ELAN520)**

Header onboard	RS232 Signal	RS485 Signal ★	D-SUB connector
Pin 1	DCD		Pin 1
Pin 2	DSR		Pin 6
Pin 3	RxD	B	Pin 2
Pin 4	RTS		Pin 7
Pin 5	TxD	A	Pin 3
Pin 6	CTS		Pin 8
Pin 7	DTR		Pin 4
Pin 8	RI		Pin 9
Pin 9	GND	GND	Pin 5
Pin10	open		

★ RS422 is optional. If you want to use RS485 you must make a short circuit between header pins 2, 4 and 6.

**X08 Serial port COM D (from 37B787)**

Header onboard	RS232 Signal	RS485 Signal ★	D-SUB connector
Pin 1	DCD		Pin 1
Pin 2	DSR		Pin 6
Pin 3	RxD	B	Pin 2
Pin 4	RTS		Pin 7
Pin 5	TxD	A	Pin 3
Pin 6	CTS		Pin 8
Pin 7	DTR		Pin 4
Pin 8	RI		Pin 9
Pin 9	GND	GND	Pin 5
Pin10	open		

★ RS422 is optional. If you want to use RS485 you must make a short circuit between header pins 2, 4 and 6.

**X09 Serial Port COM C (from 37B787)**

Header onboard	RS232 Signal	RS485 Signal ★	D-SUB connector
Pin 1	DCD		Pin 1
Pin 2	DSR		Pin 6
Pin 3	RxD	B	Pin 2
Pin 4	RTS		Pin 7
Pin 5	TxD	A	Pin 3
Pin 6	CTS		Pin 8
Pin 7	DTR		Pin 4
Pin 8	RI		Pin 9
Pin 9	GND	GND	Pin 5
Pin10	open		

★ RS422 is optional. If you want to use RS485 you must make a short circuit between header pins 2, 4 and 6.

**X10 Serial Port COMB (from ELAN520)**

Header onboard	RS232 Signal	RS485 Signal ★	D-SUB connector
Pin 1	DCD		Pin 1
Pin 2	DSR		Pin 6
Pin 3	RxD	B	Pin 2
Pin 4	RTS		Pin 7
Pin 5	TxD	A	Pin 3
Pin 6	CTS		Pin 8
Pin 7	DTR		Pin 4
Pin 8	RI		Pin 9
Pin 9	GND	GND	Pin 5
Pin10	open		

★ RS422 is optional. If you want to use RS485 you must make a short circuit between header pins 2, 4 and 6.

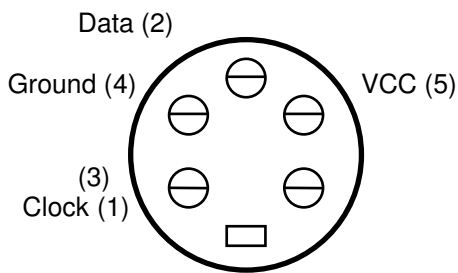
**X11 Utility Connector, PS/2 Mouse/Keyboard**

The speaker must be connected to VCC, to have a low inactive current in the speaker.

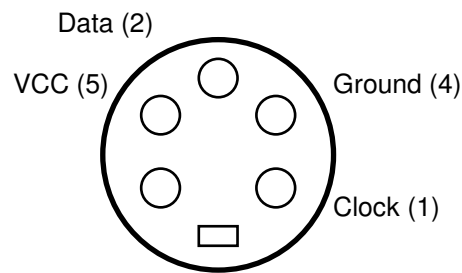
Pin	Signal	Pin	Signal
1	Speaker Out	2	Ground
3	Reset In	4	VCC
5	Keyboard Data	6	Keyboard Clock
7	Ground	8	External Battery 3.0-3.6V
9	PS/2 Mouse Clock	10	PS/2 Mouse Data

The Utility connector must be wired to a standard AT-female connector:

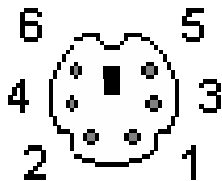
Front side AT-Keyboard (female)



Solder-side AT-Keyboard (female)



PS/2 Front side (female)



**Connector and adapter**

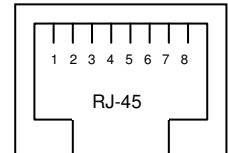
	Mini-DIN PS/2 (6 PC)	DIN 41524 (5 PC)	Remarks
Shield	Shield	Shield	KEYBOARD
DATA	1	2	
GND	3	4	
VCC (+5V)	4	5	
CLK	5	1	
	<b>Mini-DIN PS/2 (6 PC)</b>		
VCC (+5V)	4		MOUSE
DATA	1		
GND	3		
CLK	5		

**X12 USB 2 Connector**

Pin	Signal
1	VCC
2	USB-P0-
3	USB-P0+
4	GND

**X13 10/100 BASE-T Interface Connector**

X13 Pin *	Signal	RJ-45 Pin	Signal
Pin 1	TX+	Pin 1	TX+
Pin 2	TX-	Pin 2	TX-
Pin 3	RX+	Pin 3	RX+
Pin 4	RX-	Pin 6	RX-



\* These signals are ready to connect directly to a RJ-45 connector.

**X14 USB 1 Connector**

Pin	Signal
1	VCC
2	USB-P0-
3	USB-P0+
4	GND

**X15 LCD / TV-Out Connector**

Pin	Signal	Pin	Signal
1	FPM	2	FPFLM
3	Enable BKL (TTL)	4	FPLP
5	VCC-Panel 3.3V	6	GND
7	Enable VEE (TTL)	8	Shift Clock
9	Enable VDD (TTL)	10	FP0
11	FP1	12	FP2
13	FP3	14	FP4
15	FP5	16	FP6
17	FP7	18	FP8
19	FP9	20	FP10
21	FP11	22	FP12
23	FP13	24	FP14
25	FP15	26	GND
27	FP16	28	FP17
29	FP18	30	FP19
31	FP20	32	FP21
33	FP22	34	FP23
35	DVI DDA	36	DVI_DDC
37	TV-YG	38	TV-CR
39	TV-COMP B	40	TV-SYNC

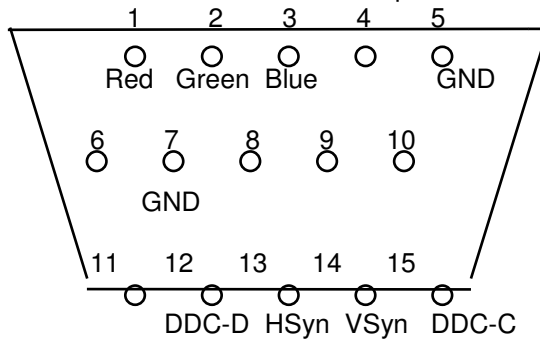
**Remarks**

Pin 9 (+12V) will be supplied from J26 (Pin 4).

**X16 VGA Monitor (CRT-Signals)**

X16 Header		15 pins HiDensity DSUB	
10 Pin -M	Signal	Pin	Signal
Pin 2	VGA red	1	Red
Pin 4	VGA green	2	Green
Pin 6	VGA blue	3	Blue
Pin 8	Horizontal Synch	13	H-Synch
Pin 9	Vertical Synch	14	V-Synch
Pin 7	DDC_DAT	12	DDC- Data
Pin 10	DDC_CLK	15	DDC- Clock
		5 + 11	Bridged
Pin 1	Ground	5, 6, 7, 8	Ground

Solderside view of the female 15pin HiDSub



## 7. JUMPER LOCATIONS ON THE BOARD

Settings written in bold are defaults!

The following figure shows the location of all jumper blocks on the MSM586SEG/SEL board. The numbers shown in this figure are silk screened on the board so that the pins can easily be located. This chapter refers to the individual pins for these jumpers.

**Be careful:** some jumpers are soldering bridges; you will need a miniature soldering station with a vacuum pump.

Top side:

Jumper	Structure	open / 1-2	closed / 2-3
J11	COM 3 RS485 settings DTR *	<b>RS232 / TTL</b>	RS485
J12	COM 4 settings (RTS) *	<b>RS232</b>	TTL / RS485
J16	COM 1 settings (RTS) *	<b>RS232</b>	TTL / RS485
J18	COM 1 RS485 settings DTR *	<b>RS232 / TTL</b>	RS485
J21	M1 VBIOS 1	<b>A17 = high</b>	A17=low
J24	CompactFlash socket select	Slave	<b>Master</b>
J28	DOC2000 select	<b>ROMCS2-</b>	C800
J32	VGA Flash enable	Disconnected	<b>Connected</b>
J33	Choose one of two VGA BIOS	<b>1.BIOS</b>	2.BIOS

\* position 2-3 only needed if the RS485 option is assembled

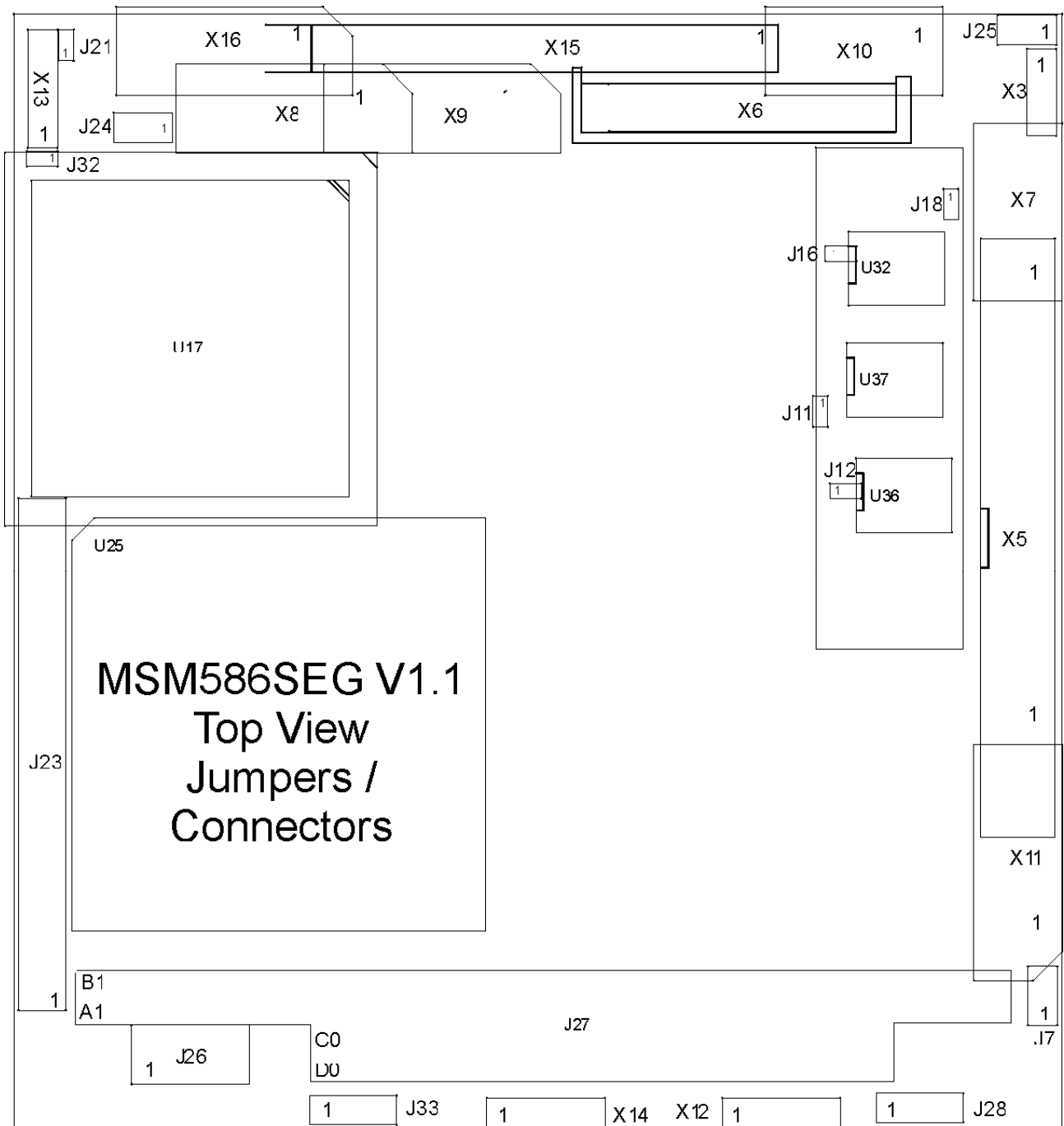
Bottom side:

Jumper	Structure	open / 1-2	closed / 2-3
J7	PowerButton	No function	No function
J8	COM 3 TTL settings RX **	<b>RS232 / RS485</b>	TTL
J9	COM 3 TTL settings TX **	<b>RS232 / RS485</b>	TTL
J10	COM 3 settings (RTS) *	<b>RS232</b>	TTL / RS485
J13	COM 4 RS485 settings DTR *	<b>RS232 / TTL</b>	RS485
J14	COM 4 TTL settings RX **	<b>RS232 / RS485</b>	TTL
J15	COM 4 TTL settings TX **	<b>RS232 / RS485</b>	TTL
J17	COM 2 settings (RTS) *	<b>RS232</b>	TTL / RS485
J19	COM 2 RS485 settings DTR *	<b>RS232 / TTL</b>	RS485
J22	M1 VBIOS 2	<b>A18 = high</b>	A18 = low
J31	LAN onboard function	<b>Open = LAN enable</b>	Closed = LAN disabled
J34	VEE	Switched	<b>Enabled</b>
J35	VBB	<b>Switched</b>	Enabled

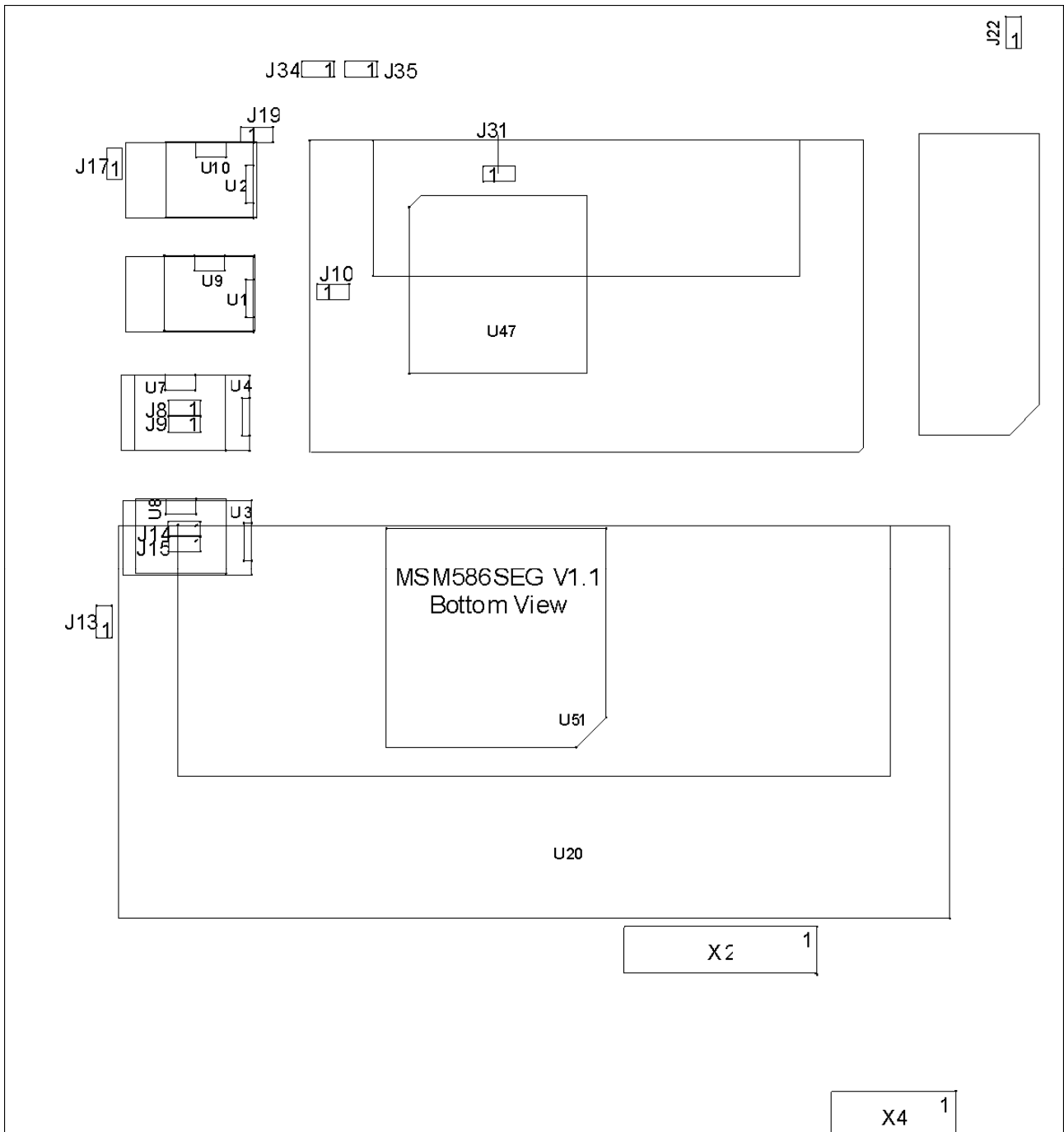
\* position 2-3 is only needed if the RS485 option is assembled

\*\* position 2-3 is only needed if the TTL option is assembled

Top side:



Bottom side:



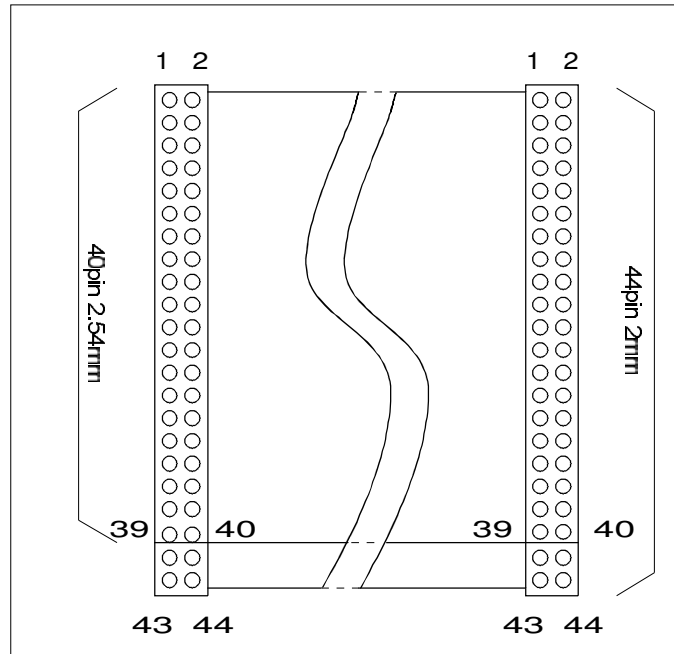
## 8. LED CRITERIA:

LED	Color	Function
D1	green	Primary HDD
D6	green	LAN active

# 9. CABLE INTERFACES

## 9.1. The Hard Disk Cable 44pin

IDT Terminal for Dual Row (2.00mm grid) and 1.00mm flat cable; 44pins = 40pins signal and 4pins power.



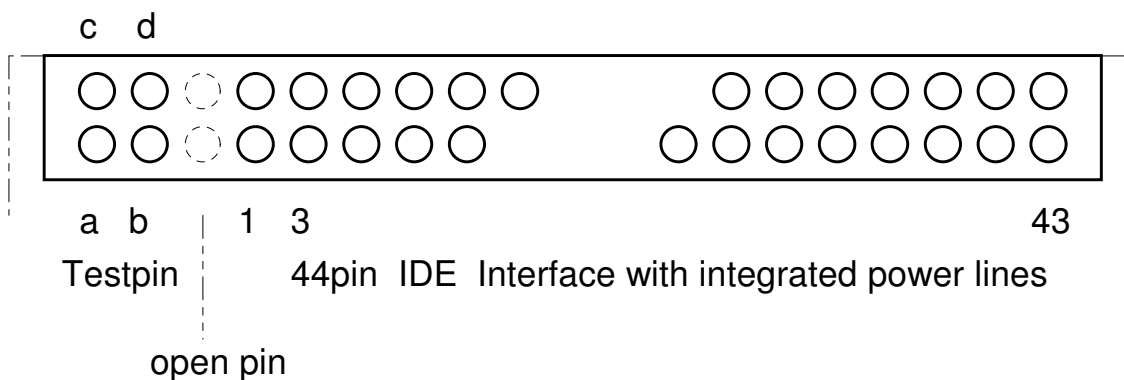
Maximum length for the IDE cable is 30cm.



**Attention!**

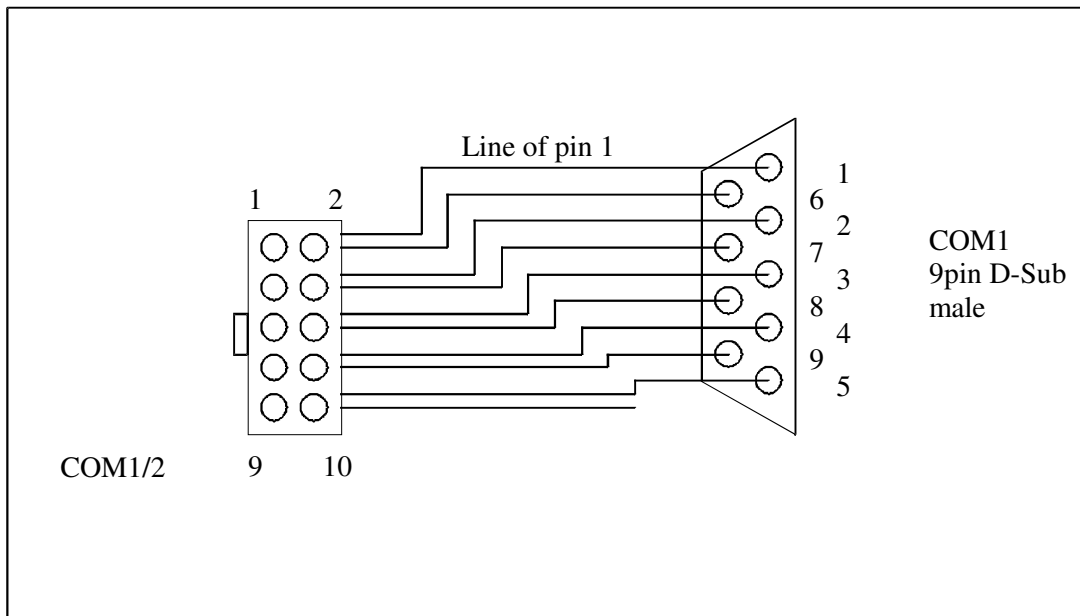
Check the pin 1 marker of the cable and the connector before you power-on. Refer to the technical manual of the installed drives because a wrong cable will immediately destroy the drive and/or the MICROSPACE MSM800SEV board. **In this case the warranty is void!** Without the technical manual you may not connect this type of drive.

The 44pin IDE connector on the drives is normally composed of the 44 pins, 2 open pins and 4 test pins, 50 pins in total. Leave the 4 test pins unconnected.



## 9.2. The COM 1/2/3/4 SerialCable

DT terminal for dual row 0.1" (2.54 mm grid) and 1.27 mm flat cable.

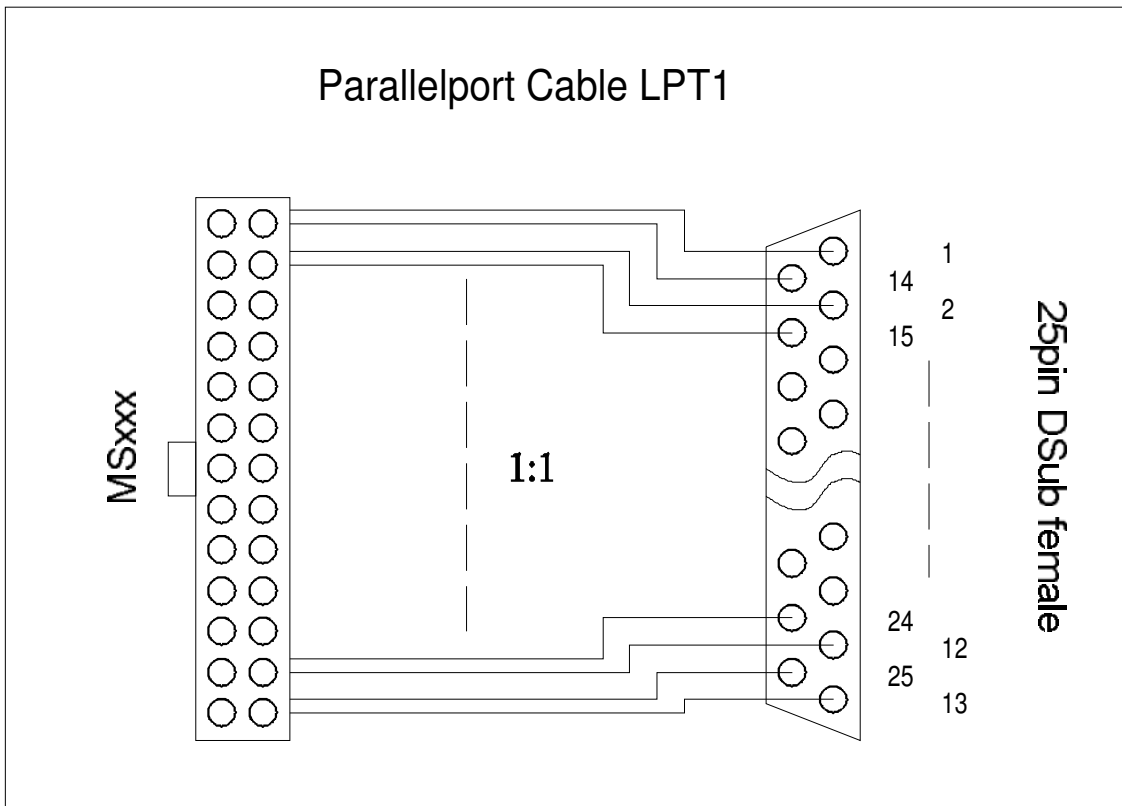


### **Attention!**

- Do not short circuit these signal lines.
- Never connect any pins on the same plug or to any other plug on the MICROSPACE MSM586SEG/SEL. The +/-10Volts will destroy the MICROSPACE core logic immediately. **In this case the warranty is void!**
- Do not overload the output; the maximum output current converters: 10mA.

### 9.3. The Printer Cable

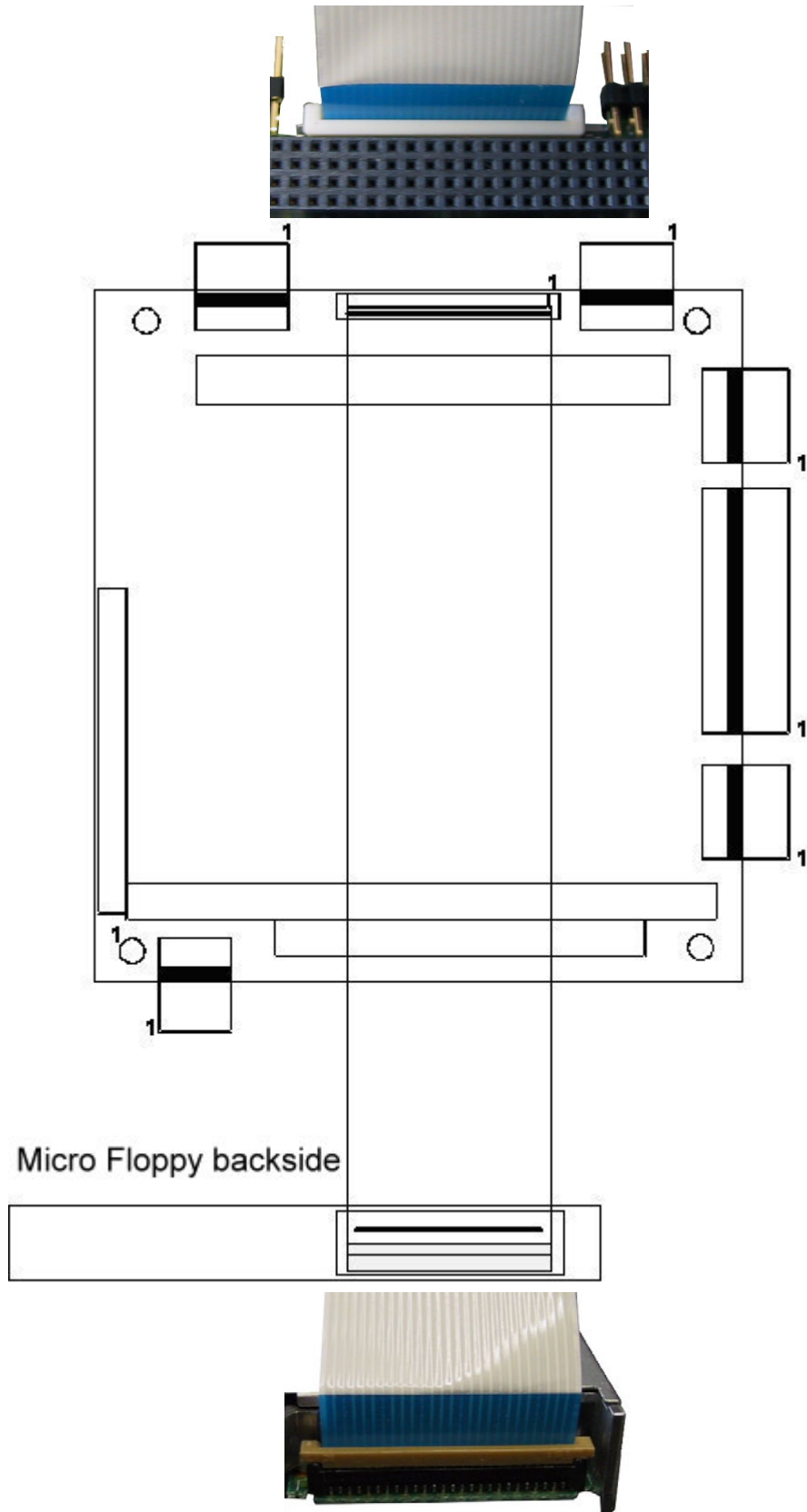
IDT terminal for dual row 0.1" (2.54mm grid) and 1.27 mm flat cable



**Attention!**

- Maximum length of this cable is 6 meters.
- Prevent short circuits.
- **Never apply power to these signals, the MICROSPACE MSM586SEG/SEL will be destroyed.**

### 9.4. The Micro Floppy Cable



## 10. SOFTWARE

On the MICROSPACE Application CD you will find all the tools and drivers you'll need to work with the card. If you are not sure about the topicality of the software, please visit our homepage to get the latest releases.

<http://www.digitallogic.com>

## 11. DRIVER INSTALLATION

### 11.1. MSDOS

#### 11.1.1. VGA Driver

Standard resolution of 480 x 640 pixels are default in the BIOS.

No other driver needed.

#### 11.1.2. LAN Driver

**Intel 82551QM Ethernet chip:**

Create a directory c:\network on your hard disk.

Copy the programs and drivers of x:\DRIVERS\NETWORK\INTEL\82551QM\ onto your HD.

#### 11.1.3. Example for MSDOS Novell 4.11

Make sure, that the following directories are in the directory c:\network:

x:\drivers\network\intel\82559er\drivers

x:\drivers\network\intel\client\dos

Create a \*.bat file in the route c:\, with the name "startpro.bat".

The file has the following contents:

```
c:
cd network
cd drivers
ls
e100bodi
ipxodi
cd.
cd dos
vlm
cd \
```

Start the file "startpro.bat".

### **11.1.4. DOC2000**

On the SSD 36pin socket a DiskOnChip DOC2000 module from M-Systems may be installed. This device is also available at DIGITAL-LOGIC AG.

#### **Operating Systems:**

DOS, DL-DOS, RTX-DOS, WIN 3.11, ROM-WIN work with these drives. All other non-DOS compatible systems need a driver.

Pay attention to the Pin 1 orientation in the 32pin SSD socket.

The latest drivers are available at <http://www.m-sys.com> .

#### **11.1.4.1. Enabling and formatting of the DiskOnChip-module**

##### **Enabling:**

No handling is needed, other than checking the jumper positions in Chapter 7.

##### **Format:**

1. Boot up from the standard floppy disk a: or from a hard disk.
2. Enter the tooldisk from M-Systems containing the format tool DFORMAT.EXE.
3. Start the format utility.  
The screen should inform you about the status of the flashdisk.
4. Enter the DOS-Bootdisk and transfer the boot files with SYS a: c:  
From this moment, the flashdisk is now the bootable drive c: and if any hard disk is connected it changes to letter D: and E:

### **11.1.5. Power Manager Driver Installation**

No driver support for DOS available.

### **11.1.6. CompactFlash (CF)**

Supported as a normal hard disk.

### **11.1.7. IrDA**

Uses COM2 supported directly through the application.

### **11.1.8. Other Driver's Installation**

No comment.

## 11.2. WINDOWS 95

### 11.2.1. LAN Driver

- Copy Intel pro95.exe driver onto the HD (x:\drivers\network\intel\82551QM\Win95\ pro95.exe).
- Extract the driver in a new directory.
- Uninstall all network drivers under Windows95 in the system and software folders and restart Windows.  
Network card Pro10 PCI will be auto-detected and all drivers can be installed (off the copied directory).

### 11.2.2. ATI M1 VGA Driver

- Put the current DLAG Product CD-ROM into the drive.
- Choose “drivers” - “VGA” in the menu (drivers\vga\ATI-M1).
- Select the setup.exe program to start the automatic driver update installation.
- Reboot the system for proper detection and activation of the new settings.

## 11.3. WINDOWS 98SE

### 11.3.1. LAN Driver

- Update the driver from the Intel pro98mem.exe device in the device manager.
- Choose the option “select list with drivers”.
- Choose the “Intel 8255xx based Ethernet PCI Adapter(10/100)”.
- Continue – if you get a failure report, press **OK**. If the PC hangs switch off/on the power.
- After rebooting you must activate the Intel 8255xx driver in the device manager.

### 11.3.2. ATI M1 VGA Driver

- Put the current DLAG Product CD-ROM into the drive.
- Choose “drivers” - “VGA” in the menu (drivers\vga\ATI-M1).
- Select the setup.exe program to start the automatic driver update installation.
- Reboot the system for proper detection and activation of the new settings.

## 12. OPERATING SYSTEMS

### 12.1. LINUX

Since we are in cooperation with SYSGO we recommend using their ELinOS Linux distribution.

<http://www.elinos.com/>

SYSGO has developed a Board Support Package (BSP) for the Pentium M and the Pentium BX/TX chipset-based products for ELinOS.

If you are interested in, or if you have any questions about, ELinOS, please contact SYSGO.

#### 12.1.1. What is ELinOS?

ELinOS is a development environment based on Linux for the creation of embedded systems for intelligent devices. With ELinOS the memory demand of Linux is reduced to less than 1MB ROM and 2MB RAM. In this manner, Linux can, for the first time, conform to the reduced hardware conditions of embedded systems. Even in this basic configuration, Linux offers largely the same functionality which made it so popular in the server and desktop field. By virtue of access to the constantly growing number of Linux components, the basic system can be expanded at any time.

The core of ELinOS is a Linux distribution custom-tailored to the embedded systems currently sold. Besides the well-known Linux version for x86, ELinOS v2.2 also supports PowerPC-, ARM-, MIPS-, and SH3-platforms which are very popular in the embedded field.

#### 12.1.2. ELinOS v4.1

The emphasis of version 4.1 is on the new CoTools, CODEO and COGNITO. CODEO is Eclipse based and provides additional plug-ins for project management and target communication, which substantially improves the ease of development of applications with ELinOS. COGNITO is a further integrated tool for the analysis of system performance. It permits the collection, recording and display of all system information and facilitates the fast optimization of software for intelligent devices.

ELinOS v4.1 has been updated to the new version of the GNU tool chain, contains the stable 2.4.31 Linux Kernel and has integration of Java and the real time extensions RTAI 3.0 for hard real time requirements. The package is complemented with Carrier Grade Extensions such as IPv6, IPSec, SNMP etc. for the use of Linux in applications in the telecommunications market.

### 12.2. Realtime OS

Must be tested carefully first. Many power management functions will control the latency time.

Contact your Realtime Operating System manufacturer and ask for the support of the Intel chipset.

## 13. BUILDING A SYSTEM

- To build up a system based on your board, you should prepare the following equipment:
- A stable power supply of 5V (> 3 ampères), depending on the CPU, memory, etc.
- Assemble the CPU with the proper clk- settings and cooling (fan) depending on the board.
- If necessary, a 12V power supply for the LCD or onboard sound.
- 8 Ohm speaker for an executed beep code (if available on the board). One may use a capacitor of 1µF connected to VCC depending on the board.
- A micro-floppy disk drive (3.5") with a PC floppy cable (26pin) or a standard FDD with appropriate cable converter. You need at least one floppy to boot the system the first time.
- A hard disk IDE 2.5" or 1.8" with the appropriate cable (44pin and 2mm grid). Do not use too long of a cable to avoid accessing problems as the IDE controller may not be able to drive the HDD.
- Connect an LCD or monitor.
- Use an AT-compatible keyboard (5 PC) or a 6 PC (PS/2) with an appropriate adapter.
- If desired, connect a mouse to it (COM or PS/2 if usable on the board).
- Connect a battery (lithium 3V or NiMH 3.6V, depending on the board) to store the data in the BIOS.
- If using SODIMMs, please refer to our overview list (also on our Product CD). Cleaning the contacts on the SODIMM and the socket with i.e., pure alcohol, is highly recommended to eliminate memory errors.



**The ELAN520 needs special SODIMMs available at DLAG.**

This information might change due to normal improvements and upgrades, please ask DLAG for the current status.

# 14. SPECIAL PERIPHERALS, CONFIGURATIONS, SOFTWARE

## 14.1. The Special Function Interface for MICROSPACE Computers SFI

All functions are performed by starting the SW-interrupt 15hex with the following arguments:

### 14.1.1. INT 15h SFR Functions

Function:	WRITE TO EEPROM		
Number:	E0h		
Description:			Writes the Data Byte into the addressed User-Memory-Cell from the serial EEPROM. The old value is automatically deleted.
Input values:	AH	78h	DLAG Int15 function
	AL	E0h	Function request
	BX		Address in EEPROM (0-1024 Possible)
	CL		Data Byte to store
	SI		1234h User-Password (otherwise EEP is write-protected)
Output values:			None, all registers are restored when reopened

Function:	READ FROM EEPROM		
Number:	E1h		
Description:			Reads the Data Byte from the addressed User-Memory-Cell of the serial EEPROM.
Input values:	AH	78h	DLAG Int15 function
	AL	E1h	Function request
	BX		Address in the EEPROM (0-1234 possible)
	SI		1234h User-Password (DLAG-Password for access to the DLAG-Memory-Cells)
Output values:	AL		Data Byte

Function:	WRITE SERIAL NUMBER		
Number:	E2h		
Description:			Writes the serial number from the serial EEPROM into the addressed DLAG-Memory-Cell. The old value is automatically deleted.
Input values:	AH	78h	DLAG Int15 function
	AL	E2h	Function request
	BX, CX, DX		Serial number
	SI		Password
Output value:			None, all registers are restored when reopened

Function:	READ SERIAL NUMBER		
Number:	E3h		
Description:			Reads the serial number from the board into the serial EEPROM
Input values:	AH	78h	DLAG Int15 function
	AL	E3h	Function request
Outputs values:	BX, CX, DX		Serial number (binary, not ASCII)

Function:	WRITE PRODUCTION DATE		
Number:	E4h		
Description:			Writes the production date into the addressed DLAG-Memory-Cell from the serial EEPROM. The old value is automatically deleted. If the Password is also in DX, the counters will be reset (=0).
Input values:	AH	78h	DLAG Int15 function
	AL	E4h	Function request
	BX, CX		Production date
	CL		Day of month (1-31)
	DI		Password (clear counter)
	SI		Password
Output values:			None, all registers are restored when reopened

Function:	READ PRODUCTION DATE		
Number:	E5h		
Description:			Reads the production date from the board in the serial EEPROM
Input values:	AH	78h	DLAG Int15 function
	AL	E5h	Function request
Outputs values:	BX, CX		Production date

Function:	WRITE INFO 2 TO THE EEPROM		
Number:	E8h		
Description:			Writes the information Bytes into the serial EEPROM.
Input values:	AH	78h	DLAG Int15 function
	AL	E8h	Function request
	SI		Password
	DI		CPU Type bits 1-7 and board type bits 8-15 (CPU type: 01h=ELAN300/310, 02h=ELAN400, 05h=P5, 08h=P3, 09h=ELAN520, 10h=P-M / BOARD TYPE ('M'=PC/104, 'E'=Euro, 'W'=MSWS, 'S'=Slot, 'C'=Custom, 'X'= smartCore or smartModule).
	BH, BL		Board Version (Ex: V1.5 => BH=1, BL=5)
	CH, CL		BIOS Version (Ex: V3.0 => CH=3, CL=0)
	DH		NUMBER OF 512K FLASH
	DL		NUMBER OF 512K SRAM
Output values:			None, all registers are restored when reopened

Function:	READ INFO 2 FROM EEPROM		
Number:	E9h		
Description:			Reads the information Bytes out of the serial EEPROM.
Input values:	AH	78h	DLAG Int15 function
	AL	E9h	Function request
Output values:	AL		Board Type BOARD TYPE ('M'=PC/104, 'E'=Euro, 'W'=MSWS, 'S'=Slot, 'C'=Custom, 'X'= smartCore or smartModule)
	DI		CPU Type bits 1-7 and board type bits 8-15 (CPU type: 01h=ELAN300/310, 02h=ELAN400, 05h=P5, 08h=P3, 09h=ELAN520, 10h=P-M / BOARD TYPE ('M'=PC/104, 'E'=Euro, 'W'=MSWS, 'S'=Slot, 'C'=Custom, 'X'= smartCore or smartModule).
	BH, BL		Board Version (Ex: V1.5 => BH=1, BL=5)
	CH, CL		BIOS Version (Ex: V3.0 => CH=3, CL=0)
	DH		NUMBER OF 512K FLASH
	DL		NUMBER OF 512K SRAM

Function:	READ INFO 3 FROM EEPROM (READCOUNTER –LOW 2 BYTE OF 3 BYTE COUNTER)		
Number:	EAh		
Description:			Reads the information Bytes out of the serial EEPROM.
Input values:	AH	78h	DLAG Int15 function
	AL	EAh	Function request
Output values:	AX		Number of boot errors
	BX		Number of setup entries
	CX		Number of low battery errors
	DX		Number of power-on starts

Function:	WATCHDOG		
Number:	EBh		
Description:			Enables strobes and disables the Watchdog. After power-up, the Watchdog is always disabled. Once the Watchdog has been enabled, the user application must perform a strobe at least every 800ms, otherwise the watchdog performs a hardware reset.
Input values:	AH	78h	DLAG Int15 function
	AL	EBh	Function request
	BL	00h	Disable
	BL	01h	Enable
	BL	FFh	Strobe
	BH		00h = BL → number of sec. / 01h = BL → number of min.
Output value:	AL	01h	Watchdog timer time-out occurred

Function:	INFORMATION ABOUT INT-15 SUPPORT ON THE BOARD		
Number:	EFh		
Description:			Gives information about the supported interrupt 15 functions.
Input values:	AH	78h	DLAG Int15 function
	AL	EFh	Function request
Output value:	BL		Function number
	SI		Password
	BX		104h or 0, if the function is not supported.
	CX	DL	

## 15. CORE BIOS SETUP

More details are available in the [separate BIOS Manual](#) on the Product CD and on DIGITAL-LOGIC's homepage.

Power-up the system and wait for the BIOS to show activity on the screen. The BIOS diagnoses the system and displays the size of the memory being tested. You may not be able to bypass the memory test depending on the BIOS producer.

### CMOS Set-up

If the CMOS configuration is incorrect, the BIOS tells you to enter the set-up screen by pressing a key. Select the correct options with the arrow keys and save them.

Function	INSYDE SOFT Keys
BIOS setup	CTRL-ALT-S
Change values	ARROWS / SPACE
Jump	TAB
Save	ARROWS
Back / exit	ESC

## 16. DIAGNOSTICS

### 16.1. Boot Loader

Checkpoint	Function Name	Function Description
00h	DIAG_SYSTEM_INIT	Boot started
01h	DIAG_A20_DISABLE	Disable A20
02h	DIAG_INIT_CHIPSET	Initialize CS
03h	DIAG_TEST_RAM	Test RAM
04h	DIAG_MOVE_BB_LOADER	Move BL into the RAM
05h	DIAG_EXECUTE_IN_DRAM	Execution in RAM
06h	DIAG_USER_FLASH_CHECK	Check OVERRIDE option
07h	DIAG_SHADOW_BIOS	Shadow System BIOS
08h	DIAG_CHECKSUM_BIOS	Checksum System BIOS ROM
09h	DIAG_NORMAL_BOOT	Proceed with Normal Boot
0Ah	DIAG_CRISIS_BOOT	Proceed with Crisis Boot
51h	DIAG_FATAL_SUPERIO	ALIM5123 not detected
0Fh	DIAG_FATAL_ERROR	Fatal Error

### 16.2. Error Beep Codes

Checkpoint	Function Name	Function Description	
F0h	ERROR_BBF_NORAM	No RAM	.... -
F1h	ERROR_BBF_RAMBAD	RAM test failed	..._ -
02h	ERROR_BBF_NOBIOS	BIOS is not shadowed	.._ -
04h	ERROR_BBF_BIOSCS	BIOS Checksum BAD	._ -
0Ah	ERROR_BBF_CRISISBAD	No CR code / CR bad	._ -

### 16.3. System BIOS in Shadow RAM

Checkpoint	Function Name	Function Description
10H	DEBUG_MISC_RESET	Some Type of Long Reset
11H	DEBUG_CS_FAST_A20_RESET	Turn off FASTA20 for POST
12H	DEBUG_POST_SIGNAL_POR	Signal Power-on Reset
13H	DEBUG_CS_CHIP_INIT	Initialize the Chipset
14H	DEBUG_OEM_ISA_VGA_SEARCH	Search for ISA BUS VGA Adapter
15H	DEBUG_HWIO_SETUP CTC1	Reset Counter/Timer 1
16H	DEBUG_OEM_SET_CMOS_REGS	User register config through CMOS
17H	DEBUG_CS_MEMORY_SIZE	Size Memory
18H	DEBUG_POST_TEST_RAM	Dispatch To RAM Test
19H	DEBUG_GEN_TEST_ROMS	Checksum the ROM
1AH	DEBUG_HWIO_RESET_INTS	Reset PICs
1BH	DEBUG_VIDEO_VIDEO_INIT	Initialize Video Adapter(s)
1CH	DEBUG_VIDEO_EQUIP_INIT	Initialize Video (6845 Regs)
1DH	DEBUG_VIDEO_COLOR_INIT	Initialize Color Adapter
1EH	DEBUG_VIDEO_BW_INIT	Initialize Monochrome Adapter
1FH	DEBUG_HWIO_TEST_DMA_PAGE	Test 8237A Page Registers
20H	DEBUG_KEYB_SELFTEST_CTLR	Test Keyboard
21H	DEBUG_KEYB_RESET_KEYBOARD	Test Keyboard Controller
22H	DEBUG_POST_CHECK_CMOS_RAM	Check if CMOS RAM valid
23H	DEBUG_POST_TEST_BATT_CMOS_SUM	Test Battery Fail & CMOS X-SUM
24H	DEBUG_HWIO_TEST_DMA_CTLRS	Test the DMA controllers

Checkpoint	Function Name	Function Description
25H	DEBUG_HWIO_INIT_8237	Initialize 8237A Controller
26H	DEBUG_POST_INIT_VECS	Initialize Interrupt Vectors
27H	DEBUG_RAM_QUICK_SIZE	RAM Quick Sizing
28H	DEBUG_RAM_PROT_ENTRY_1	Protected mode entered safely
29H	DEBUG_RAM_SIZE_DONE	RAM test completed
2AH	DEBUG_RAM_PROT_EXIT	Protected mode exit successful
2BH	DEBUG_CS_SHADOW_SETUP	Setup Shadow
2CH	DEBUG_VIDEO_EQUIP_INIT_INIT	Going to Initialize Video
2DH	DEBUG_VIDEO_BW_SEARCH	Search for Monochrome Adapter
2EH	DEBUG_VIDEO_COLOR_SEARCH	Search for Color Adapter
2FH	DEBUG_VIDEO_SIGNON	Sign on messages displayed
30H	DEBUG_OEM_CONFIG_KBD_CTL	Special initialization of Keyboard Ctr
31H	DEBUG_KEYB_PRESENT_TEST	Test if Keyboard present
32H	DEBUG_KEYB_TEST_IRQ1	Test Keyboard Interrupt
33H	DEBUG_KEYB_TEST_CMD	Test Keyboard Command Byte
34H	DEBUG_RAM_FULL_TEST	Test, blank and count all RAM
35H	DEBUG_RAM_PROT_ENTRY_2	Protected mode entered safely (2)
36H	DEBUG_RAM_TEST_DONE	RAM test complete
37H	DEBUG_RAM_PROT_EXIT_2	Protected mode exit successful
38H	DEBUG_KEYB_OUTPUT_PORT	Update OUTPUT port
39H	DEBUG_CS_CACHE_SETUP	Setup Cache Controller
3AH	DEBUG_HWIO_TEST_PERIODIC	Test if 18.2Hz Periodic working
3BH	DEBUG_GEN_CHECK_RTC	Test for RTC ticking
3CH	DEBUG_GEN_INIT_HARD_VECS	Initialize the Hardware Vectors
3DH	DEBUG_MOUSE_INIT	Search and initialize the Mouse
3EH	DEBUG_KEYB_SET_LEDS_1	Update NUMLOCK status
3FH	DEBUG_OEM_DEVICE_CONFIG	Special initialization of COMM and LPT ports
40H	DEBUG_CS_CONFIG_PORTS	Configure the COMM and LPT ports
41H	DEBUG_FLOP_INIT	Initialize the floppies
42H	DEBUG_WINI_INIT	Initialize the hard disk
43H	DEBUG_HWIO_ROM_INIT	Initialize optional ROMs
44H	DEBUG_OEM_INIT_POWER_MAN	OEM's initialization of Power Management
45H	DEBUG_KEYB_SET_LEDS_2	Update NUMLOCK status
46H	DEBUG_HWIO_FIND_80X87	Test for Co-processor installed
47H	DEBUG_OEM_LAST_MINUTE_INIT	OEM functions before Boot
48H	DEBUG_MISC_LAUNCH_INT19	Dispatch to Operating System Boot
49H	DEBUG_BEGIN_BOOT_CODE	Jump into Bootstrap Code

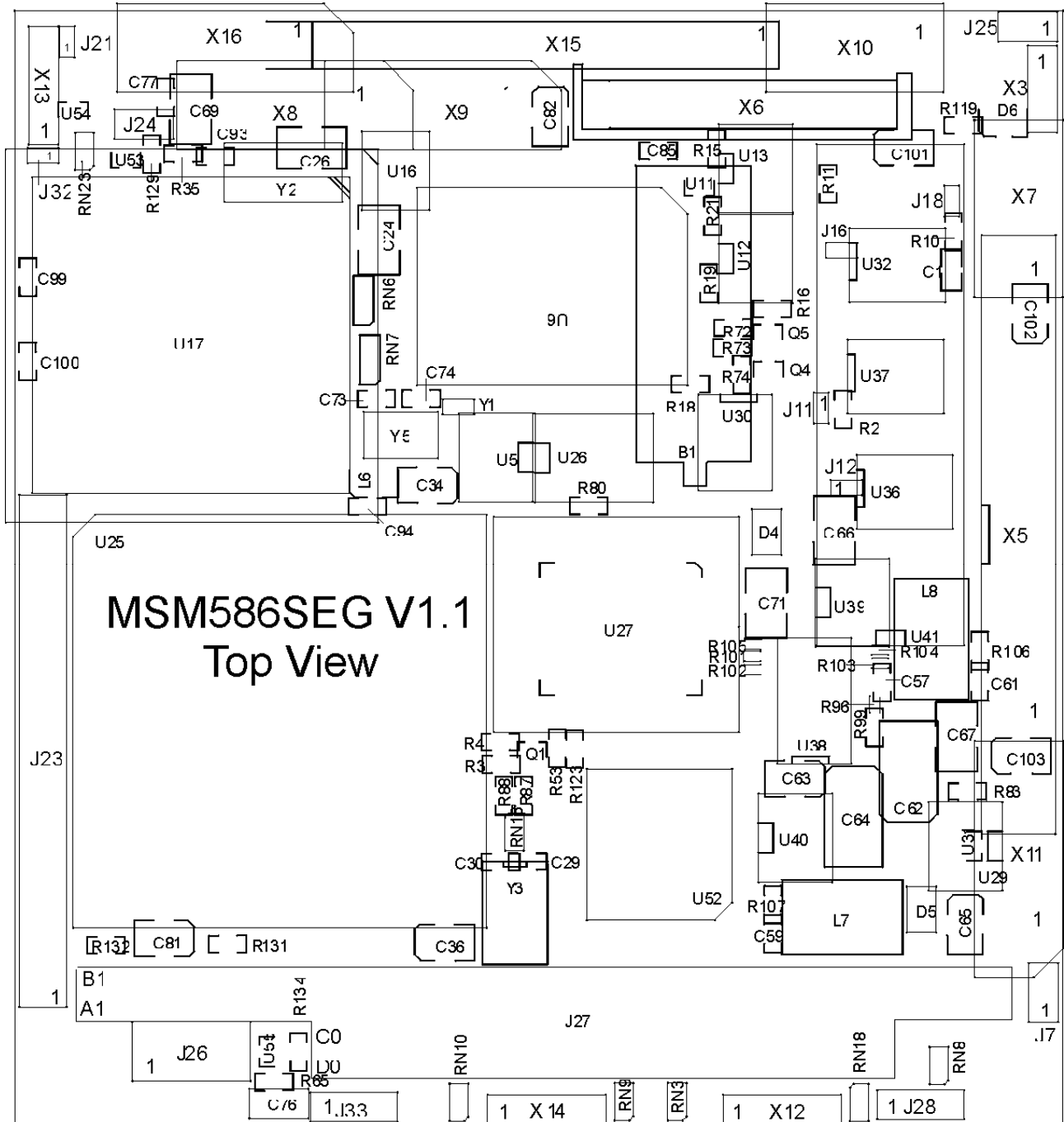
## 16.4. Error Beep Codes

	Function Description	
S = Short	S - S - S - P - S - S - L - P	The DMA page registers are faulty.
	S - S - S - P - S - L - S - P	The refresh circuitry is faulty.
	S - S - S - P - S - L - L - P	The ROM checksum is incorrect.
	S - S - S - P - L - S - S - P	The CMOS RAM test failed.
L = Long	S - S - S - P - L - S - L - P	The DMA controller is faulty.
	S - S - S - P - L - L - S - P	The interrupt controller failed.
	S - S - S - P - L - L - L - P	The 8042 keyboard controller failed.
P = Pause	S - S - L - P - S - S - S - P	No video adapter was found.
	S - S - L - P - S - S - L - P	No RAM is installed. No message is displayed.

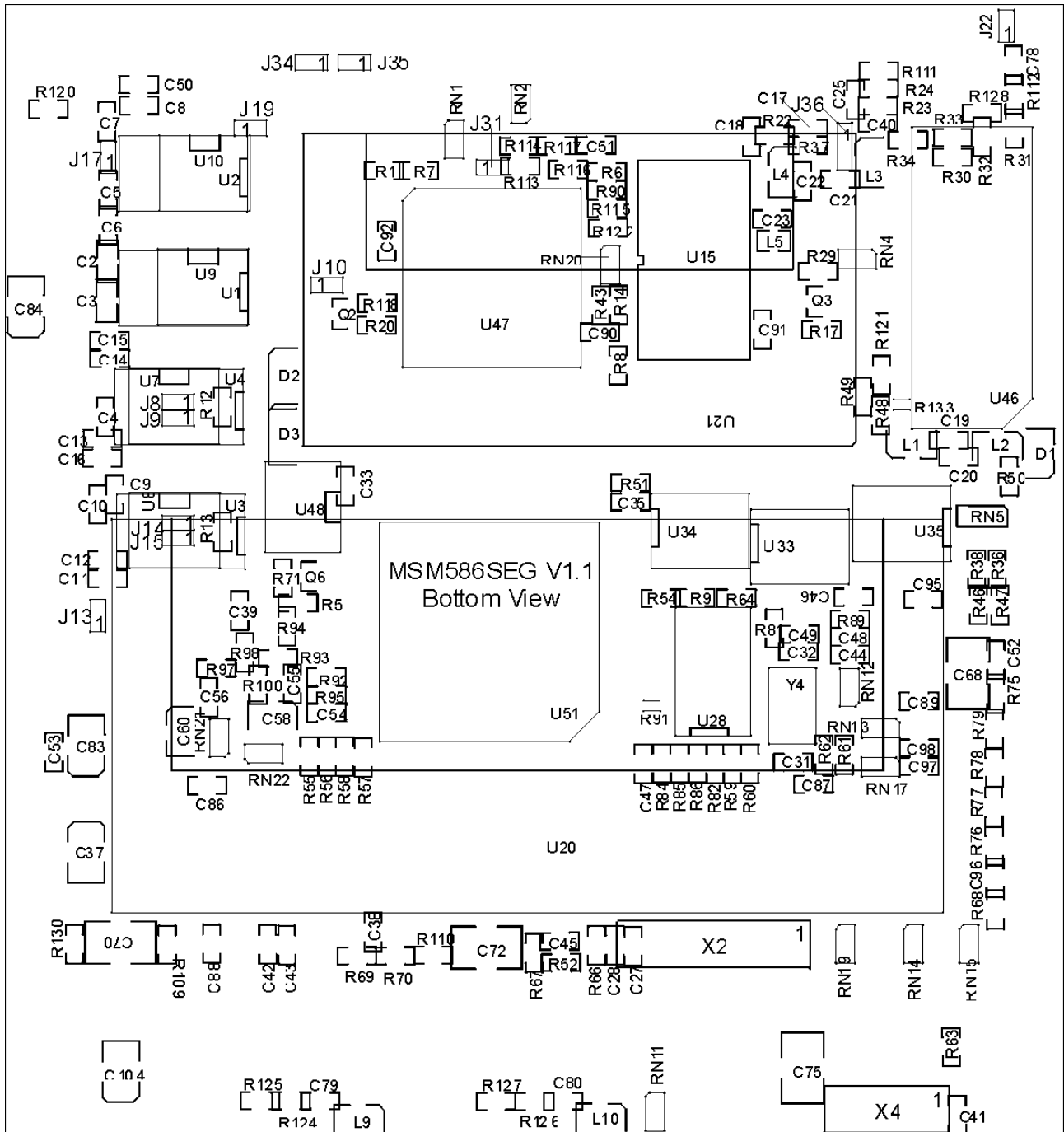
# 17.ASSEMBLY VIEWS

## MSM586SEG/SEL V1.1

### Top View



Bottom View



# 18.INDEX

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